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THE MAGAZINE FOR PROFESSIONALS

- TANDON: THE HEAD DRIVE BEHIND COMPUTER WORLD
- COMPUTER CAUSES A SEACHANGE IN CUSTOM HOUSE
- CENTRONICS BUFFER
- VHF/UHF WIDE-BAND AMPLIFIERS
- RECORDING PLAYBACK AMPLIFIER
- BATTERY 'LOW' INDICATOR

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BUDGET INDICATES NEGATIVE THINKING

Electronics industry in the country has little to cheer about in the latest budgetary proposals of the Union government. The ethos of modernisation and an all out support to computerisation, coupled with liberal policies which marked the scene a couple of years ago has now disappeared.

Contrary to the oft-proclaimed goal of bringing down the prices of television sets, an increase on excise duty on the picture tubes adds to the cost. That people having too much of an "entertainment" would not mind paying a little more is at best a cruel joke.

What if the 5 per cent hike in excise duty on computers had not been proposed, one may ask. Can't the government find that couple of crores of rupees from elsewhere, ask another. What if the duties were reduced further to promote the market, queries a third person. The answer appears to be that the government's thinking has undergone a change. The electronics industry in general and the computer industry in particular do not seem to find the pride of place as they used to be in the past. Industry sources rightly observe this trend as "negative" in nature.

However, it is reassuring to hear from the industry that despite these new imposts and consequent marginal hike in prices of end products the market for television sets and computerss may not fail.

Added to the fiscal problems is the lack of a definite direction in which the industry is to go. The lukewarm attitude of the government towards matters electronics has left the industry in chaotic condition with no clear set goals. It is high time the government machinery woke up to the need for strengthening itself to evolve suitable policies and perspectives.

Front cover

The ghostly figure, known as the Head and Torso Simulator (HATS), seen here being fitted with a telephone handset by technician Helen Christion, is used in tests at British Telecom's Research laboratories to measure sound pressure.
The tests take place in an anechoic chamber. An artificial ear on the simulator holds a miniature microphone to monitor the loudness and frequency response of the telephone.

POWER LINE MODEM

The NE5050 from Philips Components has been designed for sending and receiving data over the AC mains network, coaxial cables or twisted-pair cables. The modem described here is a mains-based application of the NE5050. It works in conjunction with an error-correcting computer program for exchanging data or remote control of equipment.

by J. Bareford

A modem (acronym for MOdulator/DEModulator) is almost invariably used where the distance between computers, or a computer and peripheral equipment, exceeds the capabilities of the well-known RS-232 interface with associated cables. In practice, this means that some sort of modem is necessary when the data rate and distance exceed 1200 baud and about 30 metres respectively. In most cases, the modem is located physically close to the computer or peripheral (sometimes it is internal to it). Modems generally use frequency-shift-keying (FSK) of a carrier to convert the logic levels received from the computer's RS-232 outlet into tones that can be carried over, say, the telephone network. In receive mode, the tones from the modem at the other end of the line are demodulated and converted to RS-232 levels for sending to the computer.

The present modem does not use FSK, but ASK (amplitude shift keying) for reasons discussed below. Similar to certain types of intercom, the NE5050-based modem is connected to the remote station via the mains network.

Background to amplitude shift keying

The mains network is by no means ideal for data communication. Impulse noise, voltage dips, line impedance modulation and high-frequency signals are but a few of the sources of interference to be taken into account. Improperly decoupled fluorescent tubes, dimmers, refrigerators and washing machines are notorious for the high levels of 'mains pollution' they cause.

Clearly, the design of a practical mains modem should anticipate high levels of interference and possible corruption of data owing to the above appliances.

In radio technology, it has been known for almost 100 years that CW (*continuous wave* or modulation type A1), or simply switching the transmitter on and off, is the simplest, yet most interference-resistent, modulation method available. Figure 1 shows how CW is used by the present modem — a 120 kHz carrier is generated and digital input data determines when the carrier is to be superimposed on to the mains lines. Collision, or more precisely *summing* of data, however, occurs when two modems connected to the network

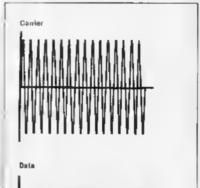


Fig. 1. The modem uses amplitude-shift keying (ASK) for sending data via the mains network.

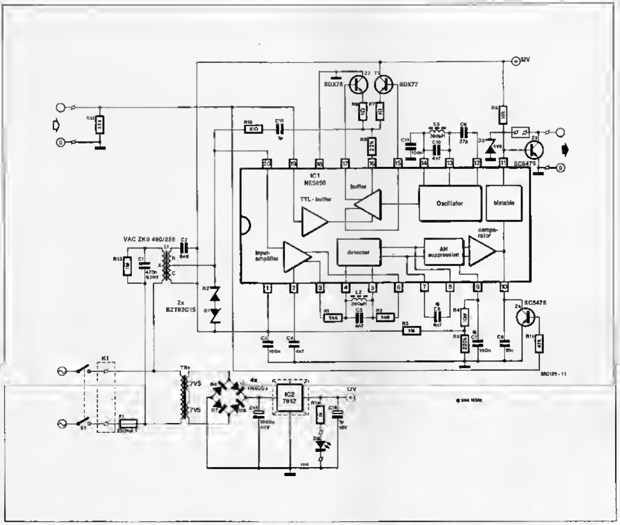


Fig. 2. Circuit diagram of the power-line modem.

transmit simultaneously. Thanks to the use of ASK, this only leads to distortion of data, not to overloading of the modem input. By setting up an error-detecting data exchange protocol in the computer, messages between modems can be repeated until they are correctly received. The use of a communications program on the computer for combatting data collision and interference simplifies the modem hardware considerably, and at the same time makes it virtually computer-independent.

An integrated modem

Apart from the electrical connection and the component values, the circuit diagram of Fig. 2 shows the internal structure of the central part, the NE5050 in position IC_1.

The transmitter in the modem chip is composed of a carrier oscillator, a TTL buffer/input amplifier, and a line driver that also functions as the amplitude-modulator. External components C_9, C_{10} and L_3 tune the oscillator to 120 kHz. Capacitor C_{11} does not form part of the tuned circuit, but serves to decouple the internally generated supply voltage of $\frac{1}{2}U_b$ which is used for biasing the oscillator. The generated carrier is applied to the line driver in which amplitude modulation takes place. The carrier is modulated by the data signal applied to pin 19 of the chip. Together with T_1, T_2, R_7, R_8 and R_9, the driver forms a class-AB output stage that gives the ASK signal enough power to be superimposed on to the mains lines. For reasons of safety, this is done with the aid of a double-insulated line transformer with a turns ratio L_{1a}:L_{1b}:L_{1c}=1:4:1. A number of components with specific functions are arranged around this transformer. C_{12} and R_{10} ensure a sufficiently high termination impedance for the line driver. C_1 suppresses the mains frequency (50 or 60 Hz), and D_1 and D_2 have the double function of transient suppressor and limiter for the received 120 kHz signal. Under no conditions should the indicated diodes be replaced by common zener diodes which these are far too slow in this application, and, therefore, unable to protect the mains modem chip from damage by voltage surges.

The input of the modem, pin 20, normally receives not only the signals from

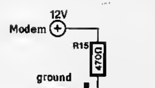


Fig. 3. Simple extension of the modem interface to enable connection to an RS-232 outlet.

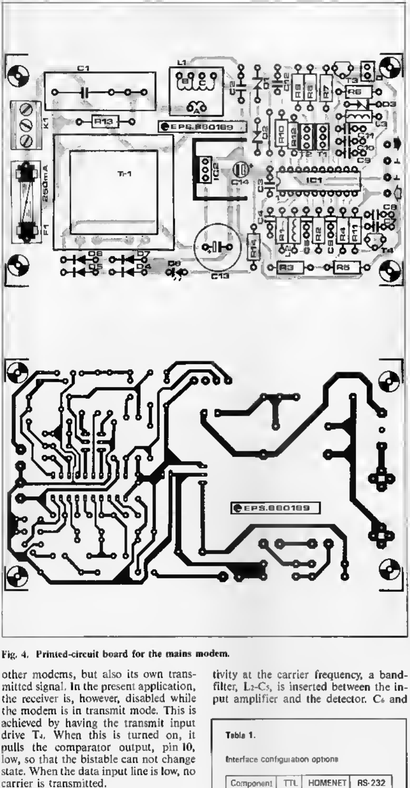


Fig. 4. Printed-circuit board for the mains modem.

Parts list

Resistors (±5%):
R_1,R_2 = 5K6
R_3,R_{13} = 1M0
R_4 = 10M
R_5 = 220K
R_6 = 10K
R_7;R_9 = 1R0
R_8,R_{12} = 22K
R_{10} = 10R
R_{11} = 47K
R_{14} = 1K0

Capacitors:
C_1 = 470n, 630 V
C_2 = 6n8
C_3;C_7;C_{11} = 100n
C_4;C_5;C_6;C_{10} = 4n7
C_8 = 10n
C_9 = 27p
C_{12} = 1µ0
C_{13} = 1000µ; 40 V; radial
C_{14} = 1µ0; 16 V; radial

Semiconductors:
D_1;D_2 = BZT03C15$^+$ (Philips Components)
D_3 = 5V6; 400 mW zener diode
D_4 . . D_7 incl. = 1N4001
D_8 = red LED
T_1 = BDX77$^+$
T_2 = BDX78$^+$
T_3;T_4 = BC547B
IC_1 = NE5050$^+$ (Philips Components)
IC_2 = 7812

$^+$ Listed by Universal Semiconductor Devices Ltd

Miscellaneous:
L_1 = VAC ZKB 490/255 (VAC Vacuumschmelze GmbH • Werk Hanau • Grüner Weg 37 • 6450 Hanau 1 • West-Germany. Tel +49 6181 362-1; telex 4184863; fax +49 6181 362645).
L_2;L_3 = 390µH
S_1 = double-pole on/off switch.
F_1 = 250 mA delayed action fuse with PCB-mount holder
Tr_1 = PCB mount transformer; 3 VA; 2×7.5 V @ 200 mA.
K_1 = 3-way PCB-mount terminal block.
Heat-sink for IC_2.
Moulded ABS enclosure, e.g. Bopla E440, or OKW A9030065.
PCB Type 880189

other modems, but also its own transmitted signal. In the present application, the receiver is, however, disabled while the modem is in transmit mode. This is achieved by having the transmit input drive T_4. When this is turned on, it pulls the comparator output, pin 10, low, so that the bistable can not change state. When the data input line is low, no carrier is transmitted.

The received signal is first applied to an amplifier provided with a band-pass characteristic. The high-frequency roll-off point is internally set to 300 kHz. Dimensioning C_4 allows defining the lower roll-off point in accordance wit the carrier frequency used. To ensure selectivity at the carrier frequency, a band-filter, L_2-C_5, is inserted between the input amplifier and the detector. C_6 and components internal to the detector create a low-pass filter for shaping and cleaning the digital pulses. This filter not only suppresses high-frequency signals, but also sets the maximum data rate — in this case, to 1 Kbit/s. Background signals at the mains frequency are rejected by the AM-suppressor. This works by storage of the average direct voltage level in C_7. When no input signal is available for more than 4 s, the voltage on C_7 would rise slowly to a value that results in a logic high level at the output. This is prevented by R_3, R_4 and R_5.

Table 1.

Interface configuration options

Component	TTL	HOMENET	RS-232
D_3	1	0	0
T_3	0	1	0
J_1	1	0	1

1 = fit component
1 = emit component

The comparator, in combination with C_8, cleans the detected pulses, whose edges are straightened again by the inter-

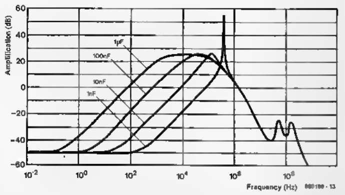


Fig. 5. Receiver amplifier gain vs frequency for different values of the high-pass capacitor.

nal bistable. This has an open-collector output that drives a simple computer interface set up around T_3. Table 1 lists the possibilities of configuring this interface in accordance with three interfacing standards. Since an RS-232 interface works with positive and negative voltage levels, the interface should be extended as shown in Fig. 3. R_{15} and R_{16} simply raise the ground potential of the interface to half the supply voltage of the modem. This results in the circuit driving the RS-232 interface in the computer with a voltage swing of ± 6 V, which is adequate for correct operation in most cases. Ground of the circuit is, therefore, not ground of the RS-232 interface. One additional resistor, R_{17}, is needed to protect the data input of the modem against the voltage levels of up to ± 12 V supplied by the computer's RS-232 driver.

Noise suppression by the modem can be improved by increasing the value of C_6 and C_8 to 10 nF and 100 nF respectively. This measure effectively results in a lower bit-rate of 300 per second, but speed up communication between modems since less information needs to be sent back and forth on account of corrupted data. Finally, some experimenting may be required with the value of C_4 — a lower value results in a narrower bandwidth of the input amplifier. Possible capacitor values lie between 470 pF and 1 nF.

Construction: safety first

For your own safety, the power line modem must never be constructed on a printed circuit board other than the one shown in Fig. 4.
Completion of the board with reference to the parts list is not expected to cause difficulty. The unit is fitted in an ABS enclosure provide with a grommet and a strain-relief clamp for the mains cord. The connector or socket for the bidirectional serial link to the computer should be located as close as possible to the rfelevant connections on the printed circuit board, so that the wires can be kept as short as possible.

One adjustment

To begin with, the data input of the modem should be held at about +5 V. This is easiest done by connecting a 27 kΩ resistor between the input and the +12 V line in the modem. Never apply power until a thorough check of the completed board, and the way it is connected to the mains, has been made.
Power up and use an oscilloscope to inspect the waveform at pin 20 of IC_1. Adjust the core in L_1 for maximum amplitude of the carrier. When an oscilloscope is not available, an analogue voltmeter may be used instead, but only if this is known to be able to work at 120 kHz in the alternating voltage range.

Sending and resending packets: enter Kermit

As already hinted at, reliable data communication with the modem can only be achieved when the computers at both ends run a communications program capable of error detection and correction. Owners of the Commodore C64 computer are advised to use General Electric's excellent program HOMENET.
The prototype of the power line modem was tested under control of the PC communications package PROCOMM version 2.4.2, whose capabilities are outstanding considering the cost. PROCOMM is set to the Kermit mode with the following line settings (ALT-P; option 7): 8 data bits; 1 stop bit, no parity; 300 baud; half-duplex and a time-out of 999 ms. In Kermit mode, PROCOMM allows the user to define the packet size. Initially, go to the Kermit setup menu, and select a small packet size to keep resending time low.
The Kermit protocol works basically as follows. The first packet sent by the computer is accompanied by a CRC byte (CRC = *cyclic redundancy check*). The CRC byte generally provides better results than a *checksum* by virtue of a different method of calculation: the checksum is obtained by addition, the CRC by division. After reception of the data in the remote computer, the CRC is checked, and a message is returned to indicate whether or not the packet has to be resent. This process is repeated, if necessary, until correct data has been received.

Once the maximum feasible parameters for data communication with the aid of the Kermit protocol are known with both modem stations, the chat mode in PROCOMM can be selected for on-line communication between connected PC stations. ■

HOMENET is a registered trademark of the General Electric Corporation. The HOMENET communications package for C64 computers may be obtained by contacting The Industry Standards Staff, General Electric Corporation, Fairfield CT 06431, U.S.A. Reference: Philips Components AN1951.

Procomm is a registered trademark of Datastorm Technologies Inc., P.O. box 1471, Columbia MO 65205, U.S.A. The latest version of Procomm is stated to cost US $35.00 including disk. Datastorm's auto-answer BBS service can be contacted 24 hours a day and 7 days a week on telephone number USA 314 449-9401.

Note: in Philips Components' *Application Note AN1951* on the NE5050, a line transformer identified as TOKO AMERICA #707VX-T1002N is recommended for 110 V mains networks.

HYBRID VHF/UHF WIDEBAND AMPLIFIERS

Recently, Philips Components have added a number of new devices to their well-established OM3xx and OM9xx ranges of hybrid wideband amplifiers made in thick-film technology. The five new integrated circuits provide a wide range of gains, and should be of particular interest for the design of VHF/UHF wideband boosters, since they require remarkably few additional components. A fully worked out application of the new chips in such a booster is included in this article.

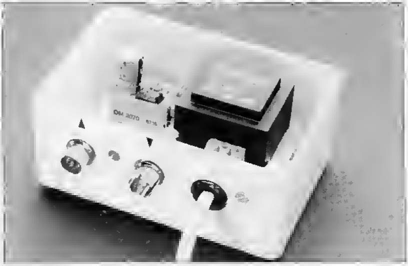
by H. Stenhouse

The new devices in Philips Components' series of integrated wideband amplifiers include a single-stage type, the OM2045 with a gain of 12 dB, a two-stage type, the OM2050 with a gain of 18 dB; and two three-stage types, the OM2060 and OM2061, with gains of 23 dB and 28 dB, respectively. All of these can be used as RF gain blocks with an input and output impedance of 75 Ω, in the frequency range between 40 and 860 MHz.

Since virtually all that is necessary for building a reliable wideband RF amplifier with good specifications is contained in a single chip, many applications are feasible. The amplifiers are, for instance, ideal for use in the domestic cable network for radio and TV, in which additional gain is often required to overcome cable losses. Radio amateurs, too, will find the amplifiers useful for general-coverage reception experiments, as the 6-m band, 2-m band and 70-cm are covered in one go. One further application is the use in 480 MHz or 612 MHz intermediate-frequency (IF) amplifiers of indoor units for satellite TV reception which incorporate a surface-acoustic wave (SAW) filter with high insertion loss.

A practical design

The circuit diagram of Fig. 1 demonstrates the simplicity of a VHF/UHF wideband amplifier set up around one of the new OM20xx types. Apart from a supply and, of course, the hybrid chip, all that is needed to obtain a complete RF amplifier are two capacitors and a small choke if a two- or three-stage amplifier chip is used. Thanks to the simplicity of the circuit, it can be housed in a compact enclosure. The supply voltage for all amplifier chips is 12 V ±10% at a maximum current drain of 110 mA (OM2070), allowing the use of a simple power supply composed of a small 15 V mains transformer, a 500 mA bridge rectifier, a



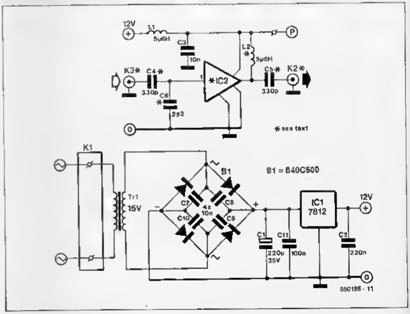


Fig. 1. Circuit diagram of the wideband aerial booster based on Philips Components' latest types in a series of hybrid amplifiers.

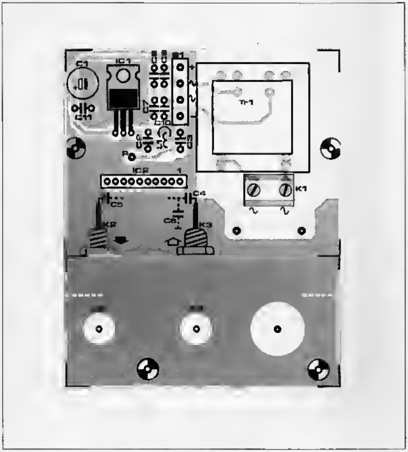


Fig. 2. Component mounting plan of the double-sided printed circuit board.

Parts list

Capacitors:
C_1 = 220µ; 35 V
C_2 = 220n
C_3 = 10n ceramic
C_4;C_5 = 330p
C_6 = 2p2
C_7 to C_{11} incl. = 100n

Inductors:
L_1 = 5µH6
L_2 = 5µH6 (see text)

Semiconductors:
B_1 = B40C500 bridge rectifier (rectangular type)
IC_1 = 7812
IC_2 = see text

Miscellaneous:
Tr_1 = mains transformer 15 V; 50-200 mA (see text).
K_1 = 2-way terminal block for PCB mounting.
K_2,K_3 = TV coax socket.
PCB Type 880186

220 µF smoothing capacitor and a 7812 integrated voltage regulator with the two usual decoupling capacitors.

Construction of the RF amplifier

The printed-circuit board shown in Fig. 2 was designed to make construction of the wideband amplifier as simple as possible, while still allowing the con-

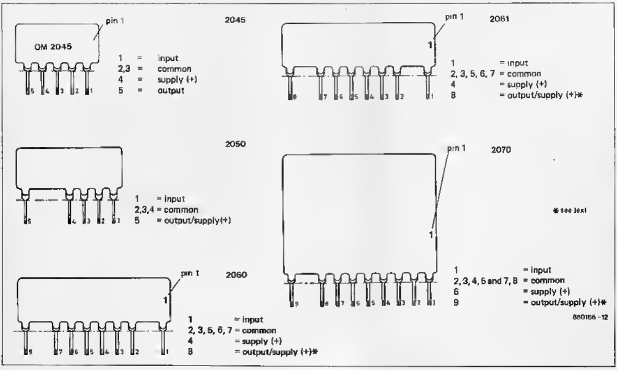


Fig. 3. Pinning of the new hybrid amplifier chips.

structor to choose and use any of the five new amplifier chips. Since the pinning of these is, unfortunately, not consistent (see Fig. 3), short wires are used instead of PCB tracks to connect input, output and supply terminals. In view of the relatively high frequencies involved, it is imperative that these wires, notably the earth connections, are not longer than 1 to 2 mm. In all cases, reference should be made to Fig. 3 to ascertain the pinning of the selected chip.

The power rating of the 15 V transformer on the PCB should be in accordance with the RF amplifier chip used — see Table 1 for the main specifications of these. When the OM2045 is used, a 1.2 VA transformer should do. The use of the OM2070, however, calls for a type rated at not less than 3.3 VA. It should be noted that some transformers require two short pieces of wire between the secondary terminals and the tracks leading to the AC connections of the bridge rectifier.

The PCB is cut in two along the dashed lines. The part with the round, etched, holes is drilled to accept the input and output sockets, and the grommet for the mains cable. After drilling, this part of the PCB is soldered vertically on to the main amplifier board as shown in the photographs. Small pieces of tin-plate are bent to shape and soldered round the input and output sockets for additional screening.

The main board may now be populated, with the exception of the amplifier chip, C_4, C_5 and C_6. The centre pin of voltage regulator IC_1 is soldered at both sides of the board.

Ten non-connected solder spots are reserved for IC_2, whose pins are connected with the aid of wires as outlined above. It is recommended to fit these connections at the reverse side of the board. The input marked *supply (+)* is connected to point P. Three ICs, the OM2060, OM2061 and OM2070, require an additional connection between the supply and the chip output. This connection is made in the form of a 5.6 μH choke between the output and point P, as shown in Fig. 4

Coupling capacitor C_4 takes the RF input signal direct from socket K_1 to the input of IC_2. The amplified RF output signal is coupled out to K_2 via C_5. To prevent stray inductance and possible oscillation, the wires of C_4 and C_5 should be kept as short as possible. Capacitor C_6 (2p2) may be added for extra suppression of interference.

Table 1.

Main technical specifications of OM20xx series.

	OM2045	OM2050	OM2060	OM2061	OM2070
U_b	12 V	12 V	12 V	12 V	12 V
$Z_i = Z_o$	75 Ω	75 Ω	75 Ω	75 Ω	75 Ω
I_c (typ.)	11.5 mA	18 mA	55 mA	50 mA	105 mA
Gain	12 dB	18 dB	23 dB	28 dB	28 dB
VSWR in	2.0	1.5	1.3	1.5	2.3
VSWR out	1.4	1.9	1.5	1.7	1.9
F(dB)	3.6 dB	5.2 dB	5.4 dB	4.4 dB	4.8 dB
U_o	99 dBμV	100 dBμV	107 dBμV	107 dBμV	113 dBμV

operating temperature: −20 to +70 °C

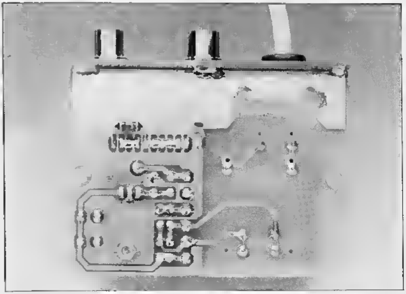


Fig. 4. Series-connected supply choke L_2 is fitted at the reverse side of the board.

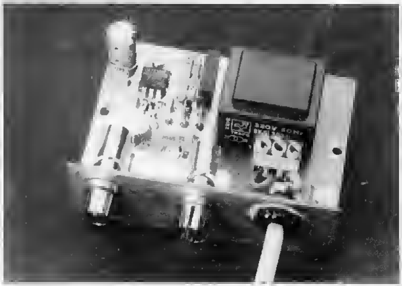


Fig. 5. Completed prototype of the wideband RF amplifier.

CENTRONICS-COMPATIBLE PRINTER BUFFER

from an idea by R. Degen

Today's computers and the programs that run on them are capable of generating massive amounts of data that is, in some way, to be put on paper. Users of computer-assisted design and engineering (CAD/CAE) and desk-top publishing (DTP) programs need not be told that the printer or plotter is almost invariably a slowing-down factor in the system. At printing time, therefore, the user is often forced to sit with his arms crossed, or go out to have a cup of tea, because the computer has insufficient memory left to store the whole of the printable file. Intermediate storage of data on disk and so-called spooler programs only partly resolve this annoying problem.
The versatile printer buffer described here is a state-of-the-art design that eliminates printer wait times. Just look at the main specifications below to convince yourself that this is your next home-made computer peripheral.

Printer wait times arise when the amount of data to be fed to the printer exceeds the free memory capacity of the computer. Today's wordprocessors, CAD/CAM/CAE and DTP programs are so large that, believe it or not, very little memory is left for the work file, be it a text, drawing or graphics image. Often, no more than a few tens of kilobytes are left of the 640 or so installed in the PC. The programs then invariably use a disk drive to temporarily store the excess data, which is 'spooled' to the printer output via the small, internal buffer and a background program. Meanwhile, however, the user can not exit the program, and further text or graphics editing may be slowed down considerably because of the spooling process.

Documentation and other text files are becoming ever larger, too. Many so-called Public Domain programs and PC utilities are accompanied by a compressed documentation file which, when de-compressed (*unpacked* or *uncrunched*) by the user, results in a printable .DOC or .MAN file of 100 kilobyte or so, which takes 15 to 30 minutes to dump on most matrix printers. Most modern matrix and ink-jet printers can be fitted with extra buffer memory, but the cost of such an extension is often quite high relative to the price of the basic printer. The most expensive of add-on buffers often provide 'only' 64 KByte, which is no great help when very large files are handled.

Printer buffer

- Centronics compatible
- Memory: user-configurable from 32 KByte to 1 MByte, or from 128 KByte to 4 Mbyte in six steps. Option to use either 32 KByte or 128 Kbyte static RAM chips (xx256 or xx1024).
- Low current consumption (40 mA) enables powering from printer. Option to use mains adapter with DC output
- Compact unit thanks to surface-mounted components
- No microprocessor
- Repeat mode: buffer does not load data while feeding printer.

A non-used character?

The present circuit is based on the fact that no printer prints ASCII character 00. In practice, the operation of the printer buffer is as follows: the computer writes data into the memory of the printer buffer. When the data flow to the printer buffer ceases, a user-defined delay is introduced before the data lines are made logic low, so that the remaining memory is loaded with zeros (00). The printable file is thus held in the printer

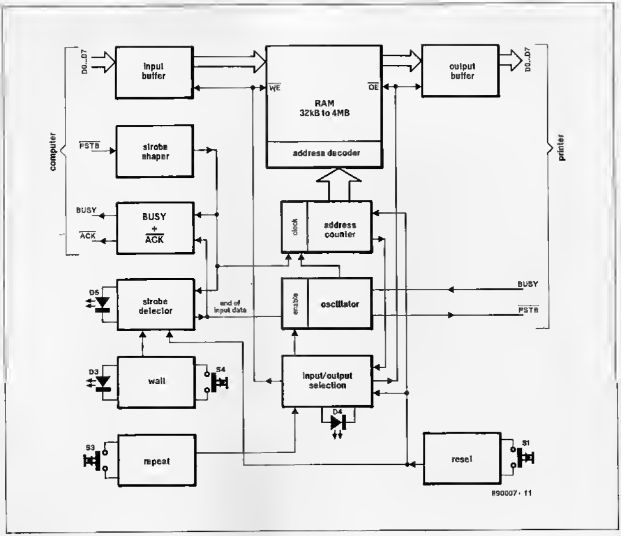


Fig. 1. Basic internal structure of the printer buffer.

buffer, and its size is known. When this process is completed, the file(s) held in the printer buffer are ready for sending to the printer. The total content of the buffer memory, including the zeros, is then fed to the printer (the zeros, of course, do not appear on paper!). The computer is called upon only when the size of the file to be loaded into the printer buffer exceeds the available storage capacity (this depends on the memory configuration selected by the user, and will be reverted to). Provided the computer has not produced a *time-out* error in the mean time, the remainder of the file is loaded after the printer has completed printing the memory content of the buffer.

Obviously, to avoid printable files being loaded in two or more passes, the buffer's memory should have capacity at least equal to the size of the largest anticipated printable file. Few problems are expected here, however, considering that 128 KByte RAMs can be fitted in the circuit. A few examples: the text file for this very article is 29,287 bytes large (WordPerfect 4.2), while the circuit diagram, originally drawn with the aid of OrCad-SDT3, takes up 360 KByte (size A3 sheet). The Postscript DTP file used for composing galley-proofs of this article with the aid of Ventura Publisher 1.2 occupies 422 KBytes. CAD programs, such as PCB design and schematic drawing packages, invariably switch the matrix printer to its graphics mode, and little needs to be said of the 'printing speed' then achieved...

Functional description of the printer buffer

The printer buffer is a relatively complex circuit and it is, therefore, useful to first get acqainted with its general structure, shown in the block diagram of Fig. 1. The function of the keys on the printer buffer is as follows:

WAIT

When several files are to be printed, the printer buffer can be switched to wait mode so that it can load all printable files in succession.

REPEAT

This key enables the buffer to print the same file more than once (copy function).

RESET

The buffer can be reset and re-initialized by pressing RESET. Internal bistables and the memory size counter are reset to zero. It should be noted that reset overrides the repeat function, so that reprintable characters in the buffer may corrupted. The RESET key should not, therefore, be actuated before the buffer has completed feeding out all of the copies selected with the repeat function.

With reference to the block diagram in Fig. 1, the central part is the buffer's memory with its associated address decoding and address counting circuits. The address counter is clocked during the loading as well as feeding out of data. Loading is clocked by the strobe pulses supplied by the computer, and feeding out by an oscillator. At the computer side, an input buffer is provided for the databits, and a clean-up circuit that shapes the strobe pulses and prevents double clocking. A third block takes care of the BUSY and ACK (acknowledge) handshaking with the computer.

The buffer loads and stores data as long as strobe pulses are applied by the computer. The strobe detect block monitors the reception of strobe pulses. When these fail, the oscillator clock is enabled, either to fill the remainder of the internal memory with zeros, or, when the memory is full, to start feeding the printer.

The block marked WAIT FOR INPUT is controlled by WAIT switch S_4 which allows the strobe detect signal to be overridden, thus forcing the buffer to load further data (but only if free memory is still available).

The functions of blocks REPEAT, IN/OUT SELECT and RESET are obvious. IN/OUT SELECT determines the data transfer direction: from computer to buffer (IN), or from buffer to printer (OUT). The databus buffers are required to ensure stable signal levels even when the maximum number of RAMs, 32, is installed.

The BUSY and STROBE signals derived from the previously mentioned oscillator control the data flow between the buffer and the Centronics input of the printer.

The circuit in detail

The above functional blocks are found back fairly easily in the circuit diagram of Fig. 2.

The input handshaking circuit of the printer buffer is composed of IC_{12} and D-type bistables FF_3 and FF_4. Circuits IC_7 and IC_8 form the address counter, and IC_{10}-IC_{11} the address decoder. The memory of the printer buffer is formed by static CMOS RAMs in positions IC_{15} through IC_{22}. Bistable FF_2 and timer IC_9 function as strobe pulse detector that determines when the file(s) has (have) been loaded completely. Direction switching (IN/OUT) as outlined above is effected by bistable FF_1 and Schmitt trigger gates N_{17}, N_{18} and N_{19}.

The central oscillator is an R-C type built around NAND Schmitt-trigger gate N_{16}. Inverters N_{11} and N_{12}, finally, supply the strobe signal for the printer.

The memory extension circuit is shown in Fig. 2b. Each extension card holds 8 RAM chips, which are either 32 or 128 KByte types. The extension(s) is/are essentially connected in parallel to the basic memory on the main board.

Timing is essential

The letters shown at a number of essential points in the circuit diagram refer to the timing diagram of Fig. 3.

Bistable FF_3 slightly lengthens the strobe signal, A, which is supplied by the computer's Centronics port, so that a well-defined rectangular signal, B, is obtained for driving gate N_{20}. This supplies the computer with handshaking signals BUSY (C) and, via N_8 and FF_4, $\overline{\text{ACK}}$ (D). Note that some computers use BUSY as the handshaking signal, others $\overline{\text{ACK}}$, and still others both. The printer buffer is compatible with all of these.

The strobe detection circuit uses a LinCMOS (*Linear Complementary Metal Oxide on Silicon*) timer Type TLC555 (IC_9) from Texas Instruments. The first strobe pulse from the computer triggers the TLC555, which drives its Q output logic high. This causes the output of inverter N_5 to go low (signal G), so that the data reception indicator, LED D_5, lights. When the strobe pulses cease, timing capacitor C_5 is charged via R_7 and preset P_1, which allows setting a delay between 5 and about 30 s. When this delay has lapsed, the voltage on C_5 resets the TLC555. As long as strobe pulses are being received, however, C_5 is discharged by T_1, so that IC_9 can not be reset.

The rising edge of signal G clocks bistable FF_2. Since the D (data-) input of FF_2 is logic high, output $\overline{Q}$ goes low. This results in the output of N_{19} going logic high (signal H). The event marks the switching over from IN (computer to buffer) to OUT (buffer to printer), and at the same time causes the BUSY line to the computer to be actuated.

After a short delay introduced by R_{12}-C_7, the oscillator around N_{16} is started. The memory space available after loading the file(s) is then filled with zeros by disabling the data input latch, IC_{12}, and pulling the datalines to the RAMs to ground with the aid of 8-way resistor network R_{18}.

When the address line selected with RAM-configuration switch block S_2 goes logic high, the outputs of FF_1 toggle. Functionally, this means that the RAM is switched over from read to write ($\overline{\text{WE}}$, signal N, is actuated). Via N_1 and N_{13}, the clocking of FF_1 also causes the address counter to be reset in preparation for the feed-out operation.

Signal P controls gate N_{18}, and so enables the communication with the printer to be established. Gates N_{18} and inverters N_{11}-N_{12} convert the oscillator pulses to strobe pulses ($\overline{\text{PSTB}}$; signal R) for the printer, which responds to them by actuating output line BUSY (signal Q). This stops the oscillator while a character is printed. When BUSY is deactuated, a new strobe pulse is generated.

Components R_{16} and C_9 delay the strobe signal briefly with respect to the selection signal, F, for the address decoding circuit. This is done to ensure that the datalines are stable when the strobe line goes low.

The next clock pulse applied to FF_1 causes this to revert to the start state, and FF_2 to be reset via C_2 and R_6. This brings the circuit back in the initial state.

The second part of the timing diagram illustrates what happens when the printer buffer is fully loaded. Bistable FF_1 takes control of the data-buffers, and switches the circuit to the OUT mode (buffer to printer). Components R_{12} and C_7 ensure correct timing of this operation, preventing loss or corruption of printable data. After printing, D_9 rapidly discharges C_7, and so prevents the oscillator from running on, which would result in the last character being printed a number of times. During this operation, the computer is set to wait when insufficient memory is available. It will be clear that fitting enough memory in the buffer is the best way to avoid this situation.

More details...

The time before the buffer starts feeding data to the printer can be adjusted with P_1 (max. 30 s). The delay can be set in accordance with the type of data sent to the printer. Graphics data, for instance, generally gives rise to a fairly heavy calculation load, so that quite some time may lapse. When the available maximum delay of 30 s is too short, or when a number of separately loaded files are to be printed in rapid succession, the buffer may be set to WAIT mode with the corresponding key. When WAIT is deactuated, the set delay is introduced again, and printing may recommence.

The RESET key re-initializes the buffer as at power-on. Printing may, of course, also be interrupted at any time by turning the printer off-line (SELECT or ON-LINE key).

Extra copies of the printout may be obtained by pressing the REPEAT key. One proviso here, however, is that the previous run was not interrupted by a reset. This is because the reset circuit works asynchronously and may, therefore, modify the memory content.

Building the printer buffer

The printer buffer is built partly with surface-mount assembly (SMA) parts.

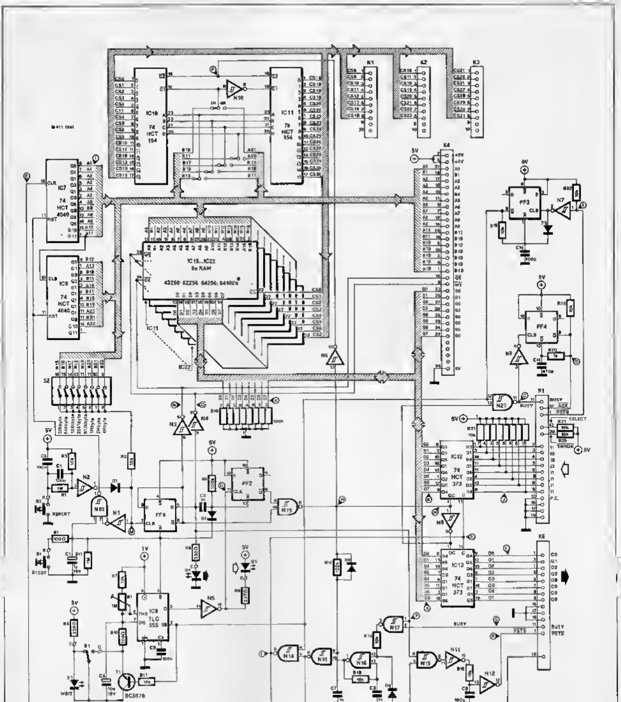


Fig. 2a. Circuit diagram of the printer buffer. The memory configuration is selected by the user.

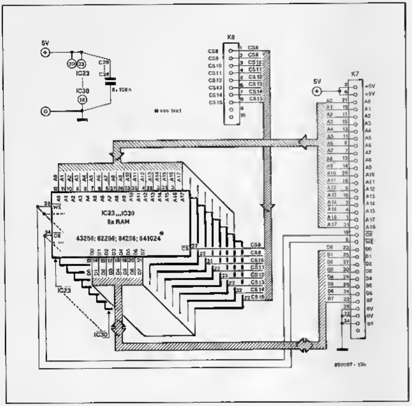


Fig. 2b. Circuit diagram of the optional memory extension board which, depending on the RAM chips fitted, provides 256 KByte or 1 MByte of additional buffer capacity.

The basic circuit is composed of two printed-circuit boards: the main board (Fig. 4a), which holds the digital control and memory circuits, and the keyboard (Fig. 4b), which holds the 3 control keys, and 4 LEDs.

Memory configuration: look before you leap

It was already noted that the user determines the memory size of the printer buffer. A third PCB is, therefore, provided as a memory extension unit (see Fig. 5) that accepts two types of static RAM: 32 KByte (43256 or 84256) or 128 KByte (841024). This third board is only required to increase the memory size of the basic printer buffer beyond 256 Kbyte (32 Kbyte chips used) or 1 MByte (128 KByte chips used.). *Attention:* it is *not* possible to mix 32 KByte and 128 KByte RAM chips. When the memory is to be upgraded, either the first choice must adhered to, or *all* chips must be removed and replaced by other types. On the PCB, there can be no doubt about the location of the chips, since 32 Kbyte and 128-KByte types are supplied in a 28-pin and 32-pin package respectively.

Five short wire links at the copper side of the PCB define the *maximum* size of the memory (either 1 MByte using 32 32 KByte RAMs, or 4 MByte using 32 128 KByte RAMs) — hence, the wire links are marked 1M and 4M. Fit the

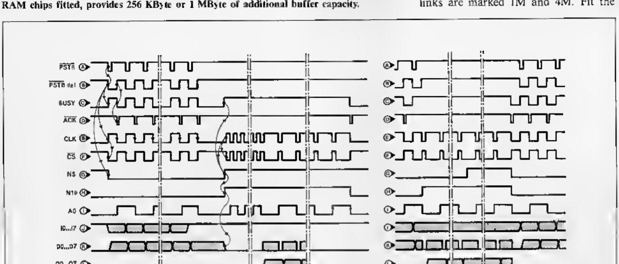


Fig. 3. Timing of the main signals in the circuit.

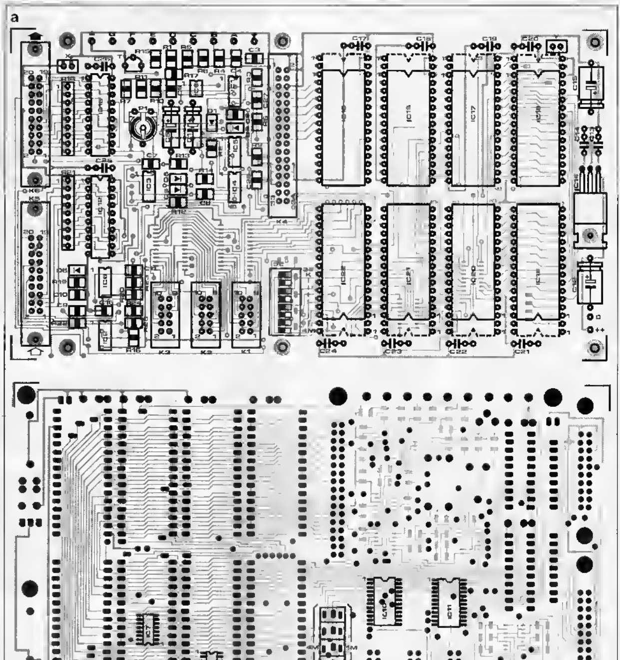


Fig. 4. Component mounting plan of the main board (4a), and the keyboard (4b).

Parts list

PRINTER BUFFER: MAIN BOARD AND KEYBOARD

Resistors (±5%):
R_{16};R_{21} = 8-way SIL resistor array 10K
P_1 = 1M0 preset H

Capacitors:
C_1 = 1µ0; 16 V
C_5 = 10µ; 16 V
C_{12} = 100µ; 25 V
C_{13} = 330n
C_{14};C_{17} . . . C_{26} incl. = 100n
C_{16} = 100µ; 16 V

Semiconductors:
D_3;D-f6-4;D_5;D_7 = red LED; 3 mm dia.
T_1 = BC557B
IC_{12};IC_{13} = 74HCT373
IC_{14} = 7806
IC_{15} . . IC_{22} incl. = 43256 (NEC) or 62256 or 84256 (Fujitsu) (32K × 8)) or 841024 (Fujitsu) (128K × 8)

Miscellaneous:
K_1;K_2;K_3 = 10-way pin header.
K_4 = 34-way pin header
K_5;K_6 = 20-way pin header.
S_1 = push-to-make button with large black cap (ITW 61-1020400)+ or Digitast.
S_2 = 8-way DIL-switch block.
S_3 = push-to-make button with large red cap (ITW 61-1020000)+ or Digitast.
S_4 = locking button with large black cap (ITW 61-2020400)+.
2 off 20-way IDC sockets.
1 off 36-way Centronics (female) connector for panel mounting.
1 off 25-way female D-connector for panel mounting.
Flat-ribbon cable as required.
Enclosure: e.g. BICC-Vero Type 4775-1410.
PCB Type 880007-1

PCB Type 890007-2

+ ITW Switches • Division of ITW Limited • Norway Road, Hilsea • PORTSMOUTH PO3 5HT. Tel.: (0705) 684971. Telex 86374 Fax: (0705) 666352.

SURFACE-MOUNT ASSEMBLY PARTS:

Resistors:
R_1;R_{10} = 100R
R_2;R_3;R_7;R_{11};R_{13};R_{14};R_{18};R_{19};R_{22} . . . R_{25} incl. = 10K
R_4;R_{17} = 1M0
R_5;R_6;R_9;R_{15} = 330R
R_8;R_{12} = 100K
R_{20} = 1K0

Capacitors: C_2;C_7;C_8 = 1n0
C_3;C_6;C_{15};C_{27};C_{28} = 100n
C_4;C_9;C_{10} = 100p
C_{11} = 470p

Semiconductors:
D_1,D_2;D_4;D_6;D_8 = BAS32 (SMA equivalent of 1N4148)
IC_1;IC_2 = 74HCT14
IC_3,IC_4 = 74HCT132
IC_5;IC_6 = 74HCT74
IC_7;IC_8 = 74HCT4040
IC_9 = TLC555 (Texas Instruments)
IC_{10};IC_{11} = 74HCT154

links marked 1M when xx256 RAMs are used, and the links marked 4M when xx1024 RAMs are used.

A dual-in-line (DIL) switch block, S_2, is used for setting the *actual* memory size. Only one switch may be closed at a time: switch 1 selects 32 KByte, switch 2 64 KByte, switch 3 128 KByte, and so on, to S_8 which selects 4 MByte. It is seen that each switch doubles the amount of memory, and extending the memory means, therefore, doubling its size (it is not possible to add, say, 32 KByte when 128 KByte is already available: the next step is 256 KByte).

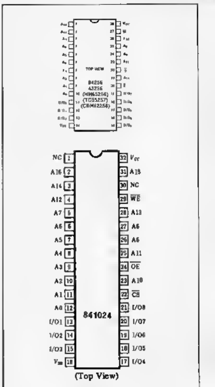
With the cost of the RAM chips in mind, the possibilities for future extensions should always be studied beforehand. For instance, for a 256 KByte configuration, there is a choice between eight 32 KByte and two 128 KByte RAMs. The latter option may currently be the more expensive, but has the advantage of allowing a future upgrade to 1 MByte (on the main board) or 4 MByte (with 3 off 1 MByte extension boards).

Fitting the SMA parts

The SMA parts are the first to be mounted at both sides of the main PCB, which is double-sided and through-plated.

There is no mystery about fitting SMA parts if a few basic precautions are observed:

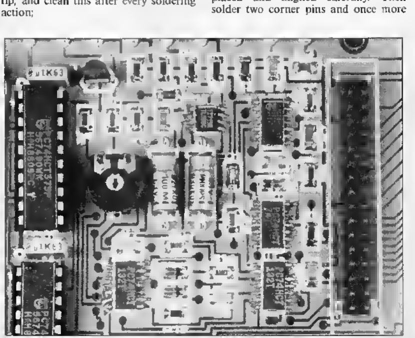
- SMA components generally do not have a printed type or value indication: therefore do not remove them from their labelled package before they are due for mounting;
- use a low-power, temperature-controlled, soldering iron with a fine tip, and clean this after every soldering action;



Pinning of static CMOS RAMs Types xx256 and xx1024.

- use thin (<1 mm dia.) soldering wire to avoid short-circuits between adjacent pins;
- solder as quickly as possible to prevent overheating the component;

SMA integrated circuits should be placed and aligned carefully. Then solder two corner pins and once more



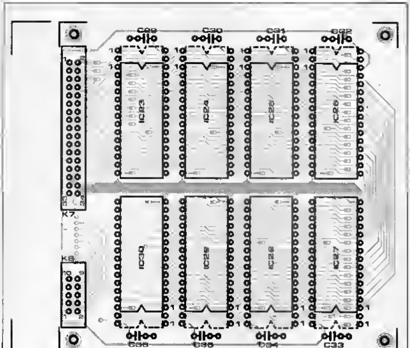


Fig. 5. Component mounting plan of the memory extension board. Depending on the memory configuration, 10-way header K_8 is connected to K_1, K_2 or K_3 on the main board.

Parts list

PRINTER BUFFFER. MEMORY EXTENSION BOARD

Capacitors:
C_{29} . . . C_{36} incl = 100n

Semiconductors:
IC_{23} . . . IC_{30} incl. = 43256 or 84256 or 62256 (32K × 8) or 841024 (256K × 8)

Miscellaneous:
K_7 = 34-way angled pin header
K_8 = 10-way angled pin header.
K_9;K_{10} = 34-way IDC socket
K_{11},K_{12} = 10-way IDC socket.
Flat-ribbon cable as required
PCB Type 890007-3

verify whether all pins line up correctly with the relevant solder islands.
For passive SMA parts, it is best to first pre-tin one of the tracks with a tiny amount of solder. Position the part, and heat the connection on the pre-tinned track. Then solder the other part connection. Again, avoid overheating and excess amounts of solder tin.

When all SMA parts have been fitted, a magnifying glass is used to inspect their connections to the tracks on the board. Also check all solder joints for possible short-circuits.

The standard parts

The first non-SMA part to be fitted is 8-way DIL switch S_2. This is mounted as an SMA integrated circuit, slightly above the PCB surface so that its pins are accessible for soldering. If changes in the memory configuration are not forseen, S_2 may be omitted: the connection that selects the relevant RAM size is then made by a wire link. Proceed with fitting the sockets for the integrated circuits, and the memory extension connector(s). The rest of the construction is entirely straightforward.
The memory extension board is not through-plated. With the exception of a number of capacitor leads, the points where through-contacting is effected are, fortunately, located well away from components. Start the construction of this board with fitting the through-contacting wires, as these are difficult to reach once the IC sockets have been mounted. A simple method of through-contacting the PCB is to temporarily insert four M3 screws with nuts in the corners of the board, so that this is a few millimetres above the working surface. Then insert the through-contacting wires vertically until they rest on the work surface. Cut off the excess wire, and solder at the top side. Once all the wires have been fitted, the board may be reversed and the screws removed. The free side of each through-contacting wire is then (quickly) soldered to the relevant spot.

Power supply

The printer buffer may be powered either by the printer or by an internal power supply. Consult the manual supplied with your printer to check whether this supplies +5 V at pin 18 of its Centronics input connector. If this is not so, wire link Y is fitted, and the 5 V regulator circuit on the main PCB is powered from a mains adapter with 8 to 12 VDC output. Wire link Y is omitted, and wire link X is installed, when the buffer is powered from the printer. When the external power supply option is used, it is recommended to connect the mains adapter via a small, 2-way DC-input socket as used on portable cassette players and some older types of pocket calculator.

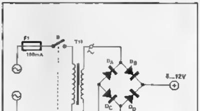
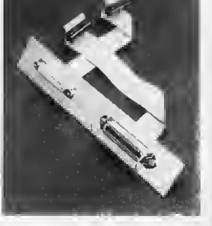


Fig. 6. Build this simple power supply if an 8 . . . 12 VDC mains adapter is not available.

Cables and connections

The main board has two 20-way pin headers for connecting the input and output cables. The pin headers mate with 20-way IDC sockets secured on to short lengths of flat ribbon cable. The input cable is fitted with a 36-way Centronics ('blue-ribbon') connector, the output cable with a 25-way D-connector. This arrangement allows the printer buffer to be connected with the aid of a pair of standard, inexpensive, printer cables.



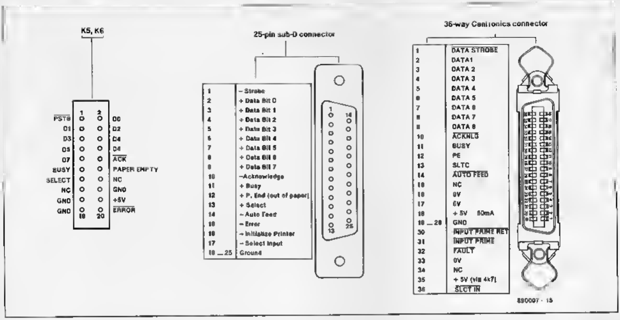


Fig. 7. Pinning of the input/output connectors, K_5 and K_6, on the main buffer, and their wiring to a 36-way Centronics input connector (input) and a 25-way female D-type (output).

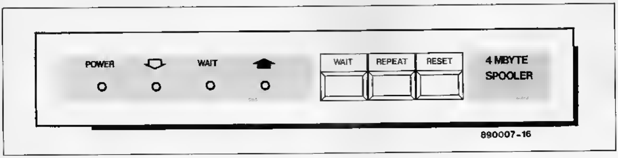


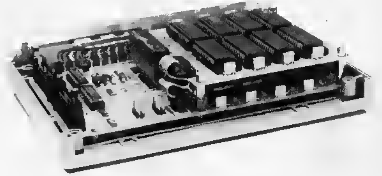
Fig. 8. Suggested lay-out of a front panel for the printer buffer.

Figure 7 shows the wiring diagram of the input and output cables. The pinning of the input and output connectors is identical. On these, the interconections are made as indicated. When a 25-way D-connector is used at the output of the buffer, pin 15 (ERROR) may be used to carry the +5 V supply voltage taken from pin 18 of the Centronics connector at the printer side.

The memory extensions are bused and connected to K_4 via a 34-way flat-ribbon cable. Each memory extension board has a 10-way pin header which is then connected to headers K_1 to K_3 on the main board, observing the logic order of the extension boards: the first is connected to K_1, the second to K_2, and the third to K_3.

The control panel, of which a suggested lay-out is given in Fig. 8, is connected to the main board via individual wires. Switch S_4 is a 2-position locking type from ITW.

The size of the control panel is such that it is easily installed vertically behind the



front panel in an ABS enclosure Type 4775-1410 from BICC-Vero. The main board and the control board are mounted on to an aluminium base plate. A drilling template for this support plate is given in Fig. 9.

Test time...

The power LED on the printer buffer should light at full intensity when the unit is switched on. If it does not, the power supply in the printer is not capable of delivering the required current, and a separate power supply should be used as discussed earlier. It should be noted that the printer buffer draws a small current from the computer via the $\overline{\text{STROBE}}$ connection. This current causes the power LED to light dimly.

Once the presence of the correct supply voltage has been ascertained, the WAIT key is pressed. The associated LED should light. Release WAIT.
Send a file to the printer buffer, which shows reception of data by lighting the input LED. After a delay determined by the size of the file, the input LED goes out. The following delay depends on the memory size, and is about 15 s with 256 KByte installed (remember that some time lapses before the non-used part of memory has been filled with zeros). The output LED will now light. Printing commences, and the output LED goes out when the print job is finished. The repeat function may now be tested. When the relevant key is pressed, the associated LED lights, and the buffer should feed out a copy of the previously loaded file. When a number of files are to be loaded for printing in one go, the WAIT key is actuated before the first file is sent to the buffer. Pressing this key remains possible until the file has actually been loaded. The WAIT key is pressed again when the last file in the batch has been sent to the printer buffer.

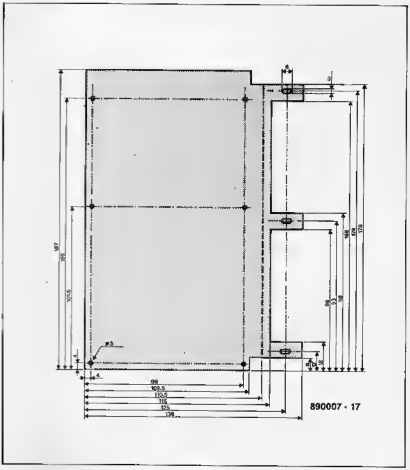


Fig. 9. Drilling template for a support bracket that holds the keyboard.

The memory configuration switch, S_2, may be replaced by a single wire link if frequent changes in the RAM size are not anticipated. Other options for this switch include an 8-way rotary type, or mounting it on to the rear panel of the printer buffer and connecting it to the main board via a length of flat-ribbon cable and a 16-way DIL header. The rotary switch is a particularly useful arrangement because it allows memory size to be reduced quickly when a relatively small file is to be loaded (because less memory is available, less time is needed to fill the non-used part of it with zeros).

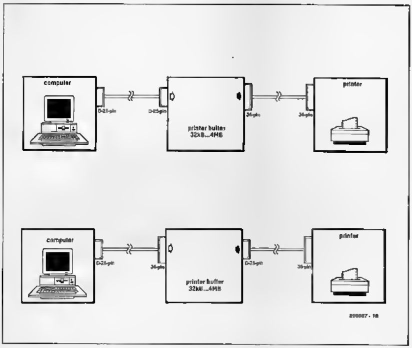


Fig. 10. Examples of how the printer buffer may be connected between the computer and the printer.

DESIGN IDEAS

COUNTER WITHOUT COUNTER

Under this paradoxical title we present a design idea for a versatile counter concept that uses an EPROM instead of the expected counter chip.

by N. Körber

The circuit described here can be configured as an up- or down-counter from 0 to 99 in BCD or 8-bit binary mode, with reset, preset and enable inputs available. All control inputs are digital compatible, allowing the user to define his own control hierarchy. Moreover, the control inputs may be active high or active low.

The counter is actuated by the positive transitions in the clock signal, and handles input frequencies well into the MHz-range. All inputs and outputs are TTL-compatible. The counter is so remarkable because its features and versatility are achieved with only a handful of commonly available components.

The Moore system

From a point of view of information technology, the present counter is similar to a so-called synchronous transforming Moore circuit. The indication *synchronous* has to do with the clock signal and the way in which the inputs are driven. A Moore circuit is a logic unit that processes input parameters x and internal conditions z to produce output states y. Each condition is associated with only one output state. As a result of input parameters and internal conditions, the Moore circuit steps through a number of states. The system not only uses currently available information, but also information acquired from past operations, whose system conditions have been recorded. A clock signal is required to switch the system to the next state.

In practice

A real Moore system is composed of a switching network and a memory. In the case of the present counter, the input parameters are the data applied to the

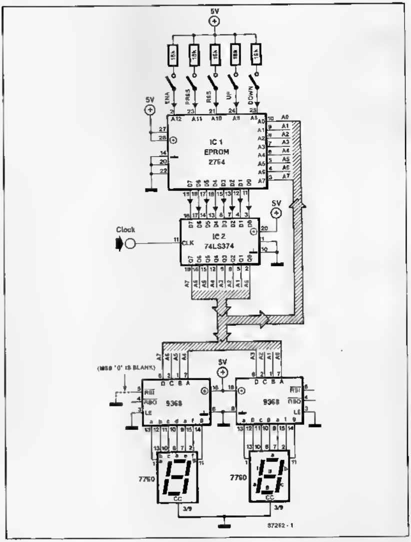


Fig. 1. Basic design of an EPROM-based counter.

control inputs. These are connected to an EPROM, which combines these data with the current conditions, to generate a system state. This state is copied into a latch (IC_2 in the circuit diagram), and so becomes the *current state*. In principle, output state *y* would then have to be generated with the aid of a further switching element. This procedure is not needed here, however, by virtue of the EPROM, which, if properly programmed, ensures that the output value (i.e., the counter state) is exactly the value that corresponds to the current state.

The operating principle of the circuit discussed here is fairly complex, but may be explained with the aid of a hypothetical circuit, based on an EPROM Type 2764 addressed between 0000 and 1FFF, that serves to count seconds pulses applied to the clock input by an external circuit.

First consider the basic timing of the events that take place in the circuit. Because switch ENA (enable) is connected to address line A12 of the EPROM, it divides the available memory capacity in two equal halves. Each of these is, in turn, subdivided in two by line A11 (switch PRESet), and again in two by the RESet switch connected to A10. For the actuation of the RESet switch to cause the displays to indicate 00, it is necessary that all memory sub-partitions addressed with A10=1 (for example, 0000 to 03FF, or 0BFF to FFFF) contain data 00.

With this in mind, and returning to the seconds counter, it is clear that 00 should be displayed when RESet is actuated. To achieve this, data available at outputs Q0 to Q7 of octal bistable IC_7 must cause the display drivers Type 9368 to drive those display segments that together form a 0.

A positive pulse transition at the clock input of the 74LS374 causes the logic state applied to each data inputs, D_n, of the chip to be copied to the corresponding output, Q_n. Assuming that the circuit is to function as a down-counter, EPROM address line A9 is made logic high by closing switch DOWN. In the 1 KByte memory area adressed, 512 bytes may be programmed such that the displayed value is decremented. Care should be taken to ensure a correct programmed sequence, since 59 must be displayed once the counter has been started.

The circuit diagram of Fig. 1 clearly shows the sub-units of the counter: the external controls in the form of switches, the EPROM, the latch circuit, and the display drivers for two 7-segment LED displays. The control parameters of the counter, ENAable, RESet, PREset and DOWN, and the current state, are applied in parallel to the address inputs of the EPROM. The EPROM uses the address so obtained to produce information on the next state. This information is made available on data outputs D0 to D7, and, a little later, on outputs Q0 to Q7 of the latch, from where it is sent to the displays. This process starts with each rising edge of the clock signal.

Programming the EPROM

The actual contents of the EPROM depend on the application of the counter circuit, and must, therefore, be provided by yourself.

The 8 Kbyte EPROM is perhaps best thought of as 8 blocks of 256 bytes. Each of these blocks is addressed by applying a particular (model-) dataword to the address inputs. When the control parameters remain umchanged, only the information applied to inputs A0 to A7 determine the output state. The changes from one state to another are a function of the preprogrammed contents of the relevant block. If, for example, RESet is pressed, the change to the next state results in the displays reading 00.

As a practical programming example, Table 1 lists the EPROM contents for a down-counter and an up-counter with 60, cyclic, states — the seconds counter discussed above. For a similar counter with, say, 100 states, the memory locations up to \$1198 have to be loaded, with \$1198 and 1199 reading 99 and 00 respectively (UP function). Similarly, the down-counter starts at \$1200 with data 99, and 98 at \$1299. Table 2 shows a further example of how the EPROM may be programmed: in this case, a two-digit decimal up/down counter is obtained. ■

Table 1. EPROM programming example for a 60-state cyclic up/down counter.

Function:	RESET
ADDRESS	DATA
\$0400 – 1FFF	00

Function: COUNT UP		Function: COUNT DOWN	
ADDRESS	DATA	ADDRESS	DATA
\$1100	01	\$1200	59
1	02	1	00
2	03	2	1
3	04	3	2
4	05	4	3
5	06	5	4
6	07	6	5
7	08	7	6
8	09	8	7
9	10	9	8
A	*	A	*
B	*	B	*
C	*	C	*
D	*	D	*
E	*	E	*
F	*	F	*
10	11	10	9
11	12	11	10
:	:	:	:
\$1159	00	\$1259	58

* don't care

Table 2. EPROM programming example for a decimal up/down counter.

Function	Address							EPROM contents	
	A12	A11	A10	A9	A8	A7 à A0		D7 à D0	
	ENA	PRES	RES	DOWN	UP	state z		resulting state	
	1	*	0	0	1	0000	0000	0000	0001
Count up	1	*	0	0	1	a	b	a	b+1
	1	*	0	0	1	a	1001	a+1	0000
	1	*	0	0	1	1001	1001	0000	0000
	1	*	0	1	0	0000	0000	1001	1001
Count down	1	*	0	1	0	a	0000	a−1	1001
	1	*	0	1	0	a	b	a	b−1
reset	*	*	1	*	*	****	****	0000	0000
	0	0	0	*	*	i		j	
Preset	0	1	0	*	*	****	****	j (don't care)	
all other bit combinations						i		j	

* = don't care

THE DIGITAL MODEL TRAIN — PART 2

by T. Wigmore

The second part in the series describes a locomotive decoder that is constructed in surface-mount technology. In conjunction with the associated digital control system, it enables up to 80 trains to be controlled independently. The associated control system will be described in a future article, but in the mean time the present decoder may be used with the Marklin digital system or any two-rail model track.

The use of surface-mount techniques (SMT) makes it possible to construct a locomotive decoder from standard components that is compact enough for fitting into a locomotive. These techniques are undoubtedly new to many readers, but this article will show that there is no real mystique about them.

The present decoder enables both a.c. and d.c. locomotives to be controlled independently of one another. In its simplest form, it is suitable for use on tracks with a centre rail (Marklin or Trix, e.g.) or with an overhead power line. The addition of the two-rail adaptor discussed later in the article enables the decoder to be used with other model railway systems. It should be noted, however, that although the decoder is compact, it can not be fitted in locomotives smaller than HO.

In Marklin stock, the space for the decoder board is ensured, because the change-over relay may be removed. This is possible, even desirable, since the decoder enables a change of direction (and the consequent switching of the head and tail lights) to be effected electronically.

As already stated, the decoder may be used with a.c. as well as d.c. systems. It is thus possible to convert a d.c. locomotive for use on an a.c. track by providing it with a slip contact and the present decoder.

In principle, it is also possible to use a Marklin locomotive on a track of different manufacture. If, however, that track is a two-rail system, the wheels of the locomotive must be electrically separated and provided with appropriate contacts. Moreover, if a two-rail track is used, the adaptor described later is also required. Although possible, this conversion is, therefore, in general not practicable.

The two-rail adaptor is also constructed in surface-mount technology and may be mounted on to the decoder. The resulting sandwich is only 2.5 mm thicker than the decoder board by itself. The use of the two-rail adaptor makes the locomotive decoder independent of the polarity of the supply and data connections. As an aside, this also solves the eternal problem of reversing loops.

- independent control of up to 80 locomotives
- may be driven by Marklin HO system or Elektor Electronics Digital Model Train System
- suitable for a.c. and d.c. locomotives
- suitable for three-rail system or, with optional adaptor, for two-rail systems
- motor current max 1 A (peak 1.5 A)
- protected against thermal overload
- speed controlled in 16 steps
- automatic change-over of independently lit head and tail lights
- lamp voltage 10 V or 20 V as required
- optional: memory from external buffer capacitor
- compact dimensions through surface-mount technology:
  35 × 24 × 7.5 mm (decoder only)
  35 × 24 × 10 mm (with two-rail adaptor)

Table 2. Technical data of the locomotive decoder.

Compatibility

Apart from the possibility of its use in a large variety of locomotives, the decoder may be operated with a number of control systems. In this context, it is perhaps of interest to know that it was designed originally and solely as part of the Elektor Electronics Digital Multi-train System which will be described in this series of articles. However, with a few simple changes (such as the baud rate), it also proved usable with the Marklin digital HO system. It is, of course, important to differentiate between the Marklin decoders and the present one.

In view of the required compactness of the decoder, the spare function offered by Marklin has had to be sacrificed in the present decoder (see Fig. 14). Marklin uses the lowest speed step (binary 1000) for reversing, assuming that this step will not be used in practice, since the motor does not operate smoothly at this (average) low voltage.

To use this voltage for reversing the direction of travel, it has to be decoded and then used as the clock signal for a bistable. In the present decoder, this

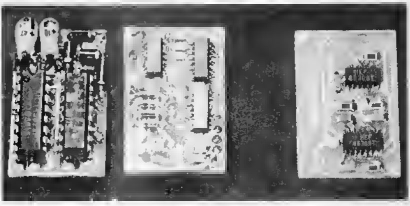


Fig. 11. The locomotive decoder is populated with mainly conventional components at the component side and with surface-mount ones at the track side to give a compact unit. At the right of the picture is the single-sided PCB for the two-rail adaptor that uses only surface-mount components.

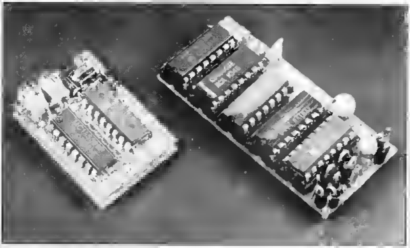


Fig. 12. At the left the prototype locomotive decoder and two-rail adaptor sandwiched together. At the right a locomotive board constructed with conventional components, which is evidence of the space saving afforded by surface-mount techniques.

would have required two additional ICs, which would have made the board too large. Fortunately, in most cases the spare function is not required anyway. Where it is needed, there is no alternative to using a Marklin decoder.

Note that if the present decoder is driven via Control 80 of the Marklin system, the spare function is used for reversing.

A more important difference between the Marklin decoder and ours manifests itself if locomotives converted for use in a digital system are run on conventional (non-digital) tracks. The Marklin decoder may be used with conventional control systems, i.e., the speed may be varied according to the amplitude of the (alternating) supply voltage and the direction of travel may be changed by an over-voltage pulse of not less than 24 V. The present decoder does not offer these facilities: in fact, a 24-V pulse (in practice, this value is normally considerably higher) would probably put paid to the power stage. It is therefore strongly recommended to use the decoder only with digital tracks.

Furthermore, the present decoder does not support Fleischmann's digital FMZ system nor that from Trix. However, locomotives in those systems (and most others) may be converted with the present decoder to make them suitable for use in multi-train set-ups. It will then depend on the rail system whether, apart from the locomotive decoder, the rail adaptor is also required.

Start at the beginning: the rails

The most important difference between a digital model railway and a conventional one is that in the former, just as in real railways, the rails carry a constant voltage. To prevent that in these circumstances all locomotives on the track travel along at full speed, they are all fitted with a decoder and a speed controller. In other words, as in real life, the speed of the locomotive is varied on board, just as if it had an engine driver. The instructions to the "engine driver" emanate from a central control, which in turn is controlled by a number of independent drive units or a computer.

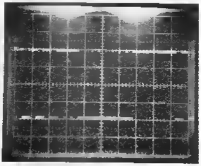


Fig. 13. The track voltage in a digital model railway systems is switched between −20 V and +20 V to ensure that the control instructions reach the locomotives via the rails in a serial data format. The locomotive power is obtained by rectifying this alternating voltage.

The instructions from the central control are transmitted to the locomotives by switching the supply voltage between +20 V and −20 V. The voltage on the rails is thus an alternating one, but it has a d.c. component whose value depends on the transmitted data.

Each period contains 18 "marker" pulses; each of the nine pairs of pulses defines a bit with three possible states: 00 = logic 0; 10 = logic indeterminate; 11 = logic 1. In this way, 9-bit words are formed; the first four are interpreted by the decoder as address and the other five as data. The logic indeterminate state is used only for forming addresses; the five data bits use only logic 0 and logic 1.

Not only locomotives, but also turnouts (points) and signals may be controlled via the rails. Normally, locomotives are addressed constantly so that they exhibit real-time behaviour. The response time of the system becomes gradually longer as more locomotives are taken into use. An added advantage of the constant voltage on the rails is that permanent lighting of the train is possible without any difficulty. This applies, of course, also to the head and tail lights, even when the train is at standstill.

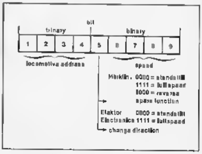


Fig. 14. The data bytes for the locomotives consist of nine bits. The first four bits form a trinary locomotive address. The other five are data that enable direction, speed and — in the Marklin system — a spare function to be controlled. One data byte is 3.8 ms long.

Block diagram

The operation of the locomotive decoder may be seen from the block diagram in Fig. 15. The rail voltage is full-wave rectified to create a supply for the power stages. Since the rail voltage is a square wave, the resulting d.c. is very pure, i.e., it has virtually no ripple. A lower direct voltage for the logic circuits is derived from the supply for the power stages.

The serial data are translated by a special decoder. These data are transmitted direct by the 'red' power line in three-rail systems or processed by the two-rail adaptor in two-rail systems. The trinary address part (first four bits) is compared with the address set on the decoder. If the two match, the next five data bits are accepted immediately. When the same five data bits have been received twice in succession, they are accepted as true and placed in the output latch.

Four of the five available data bits are used for operating the 16-step speed control; the fifth determines the direction of travel.

The speed is set with the aid of a digital pulsewidth modulator (PWM). The modulator consists of a four-bit counter with oscillator and a four-bit comparator. The counter (port A of the comparator) runs constantly. The four bits of the speed control are present at port B. Depending on the number at port B, the duty factor of the output signal varies between 0 and 15/16 at a frequency that

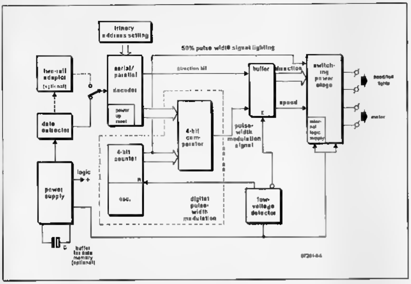


Fig. 15. The block diagram of the locomotive decoder.

is 1/16 of the counter frequency.
The PWM signal drives the output stage. Between this stage and the motor there is a fullwave rectifier. The polarity of the resulting direct voltage depends on the direction bit. This bit also serves to change over the head and tail lights that are driven by two half-wave circuits.
The lighting voltage may, if desired, be halved with the aid of a square-wave signal.
An undervoltage detector completes the set-up. If the supply voltage drops below a certain value, for instance, because the locomotive is travelling over an unpowered length of track, all signals are disconnected from the power stage and the logic circuits are set to the low-power state. In this state, the logic circuits are able to store the last received data for a short time, thanks to an optional external buffer capacitor. When the supply voltage recovers, the locomotive travels on at the last set speed.

Circuit description

In the circuit diagram of Fig. 16, the data decoding is carried out by IC_1, an MC145029 of the same family as the MC145027 used in the turnout and signal decoder described in Part 1 of this series. The significant difference between these two circuits is that in the former bit 5 is a data bit, while in the latter it is an address bit.
With the aid of wire links, a locomotive address may be set at address inputs A_1-A_4: more about this under 'construction'.
Network R_1-C_1 sets the baud rate of the decoder as required for the locomotives, while R_2-C_2 serves to detect the intervals between the data bytes.

Four of the data bits are fed to the four-bit comparator; the fifth, which, owing to N_1, is also available in inverted form, is used to change over the direction of travel and the lights via N_3, N_4 and the power stage. The counter with integral oscillator, IC_2, is designed so that the frequency of the MSB (Q_6 in this case) is about 140 Hz, which is also the frequency of the PWM signal (output of IC_3). This frequency was chosen because it will not cause undue problems owing to the self-inductance of the motor: higher frequencies may limit the motor current.
The power stage, IC_5, is a Type L293 from SGS. This chip contains four half-wave circuits, of which two may be combined into a full-wave bridge for bipolar motor control. The other two are used for the head and tail lights; these may therefore be switched relative to either earth or the positive supply line.
Gate N_2, R_6 and R_7 form the undervoltage detector. If the supply voltage

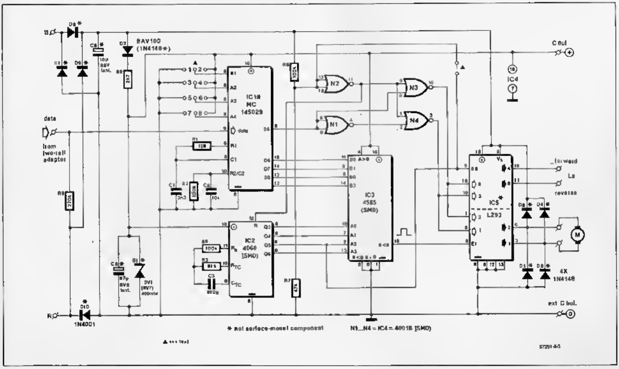


Fig. 16. The circuit diagram of the locomotive decoder.

drops below 8 V the potential at junction R_6-R_7 is interpreted by N_2 as a logic 0. This causes the reset input of the counter to become active, and this results in the PWM signal going low and the internal oscillator being stopped, which limits the current consumption.
At the same time, the remaining inputs of IC_5 are made logic 0 via N_3 and N_4. This is necessary to protect the chip (since its power supply is cut off) and to limit the current provided by the logic circuits.
The supply for the logic circuits in IC_5 is derived direct from the main power supply, because these circuits draw a fairly large current. When the main supply is present, the potential at junction R_6-R_7 is limited by the clamping diodes on board N_2 to a value that is slightly higher than that of the supply voltage for the logic circuits. If required, the E_2 input of IC_5 may be connected direct to this junction. In that case, virtually the full supply voltage is available for the lights. Since that voltage is fairly high (20 V), the E_2 input is fed with a 280 Hz square wave, which causes the effective voltage for the lights to be reduced to 10 V.
The main supply is obtained by full-wave rectification in D_7-D_{10} of the a.c. on the rails. Capacitor C_4 ensures continuity of the supply during the zero crossings of the rail voltage and blocks the counter emf generated by the self inductance of the locomotive motor when this is switched off (remember, the motor is pulse driven). A bonus of free-wheeling diodes D_3-D_6 that act in conjunction with C_4 is the virtual elimination of wheel sparking. This in turn means less interference in the electronic circuits and less contamination of wheels and rails.
The lower supply voltage for the logic circuits is derived via D_2, R_8, D_1, and C_5. This voltage must lie between 3V and 6.3 V (which is the maximum permissible input voltage of IC_5). The value chosen in the present circuit is 5.5 V because that is the rating of the possibly required external buffer capacitor. If the supply fails, and C_5 is retained as the only buffer, the circuit stores the last received data for about 5—10 seconds. This period is determined primarily by the current drawn by IC_1 (25-50 μA) and the leakage current through D_1. The use of an external buffer capacitor lengthens the period and this may be essential where locomotives are used in conjunction with the Marklin digital system and a track with conventional block protection.

Two-rail adaptor

Since Marklin uses a three-rail system, it is always clear which of the connections in the locomotive are the brown lines (outer rails) of the system and which the red line (centre rail). This is not so in two-rail systems, where the polarity of the supply lines can be reversed by reversing the locomotive. This is immaterial with regard to the main power supply, but it causes complications as far as the data are concerned.
In the Marklin system, data are present on all three lines, but those on the red line are inverted with respect to those on the brown lines. The two-rail adaptor determines which is the red line and which are the brown lines and inverts the data where necessary.
The circuit diagram of the adaptor is shown in Fig. 17. Multivibrator MMV_1 detects the intervals between the data bytes. If its input is logic high during the interval, the connected supply line is brown, the data on which must be inverted. This is done by retriggering MMV_2 at the start of the next data byte which causes N_4 to (continue to) work as an inverter.
If the supply polarity changes, the red line is connected to the input of MMV_1, MMV_2 is no longer retriggered, and N_4 ceases to invert the data.
If the supply polarity changes at precisely the time a byte is transmitted, the data comparator in the locomotive decoder prevents the acceptance of a partially inverted byte.
The supply for the two-rail adaptor is derived from that of the locomotive decoder.
The construction of the locomotive decoder and two-rail adaptor will be described in next month's instalment.

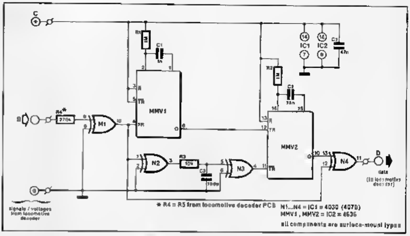
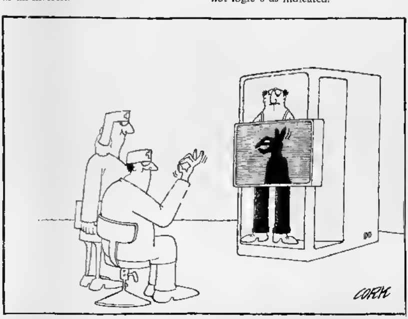


Fig. 17. The circuit diagram of the two-rail adaptor.

Corrections

In the parts list of Part 1 T_1, a Type BC547 is omitted.
In Fig. 8, bit 9 at the top is logic 1 and not logic 0 as indicated.



PRACTICAL FILTER DESIGN (3)

by H. Baggott

A practical filter may be designed in a number of ways. It may be a passive type, constructed from resistors, capacitors, and inductors, or it may contain active components that take the place of inductors. Both these types are considered in this third part in the series.

The design of a practical filter depends on the requirements, the application and the available components. Simple filters are normally designed as passive types. None the less, complex filters may very well be of the passive type also, although the size of the necessary inductors is often a severely limiting factor. Since the value of inductors for low-frequency filters is often quite high, the modern tendency is to use active filters for low-frequency applications. However, cross-over filters for use in loudspeaker systems are often still of the passive type. In this article a number of filter designs complete with formulas for their practical realization will be described. These considerations will be confined to low-pass sections, since these form the basis of all other types. High-pass filters are a direct derivative of low-pass sections, while band-pass networks with a fairly wide response are constructed from a mix of low-pass and high-pass sections. Band-pass filters with a narrow response and all-pass filters will be considered later in the series.

Passive low-pass sections

Two versions of passive low-pass section will be considered:

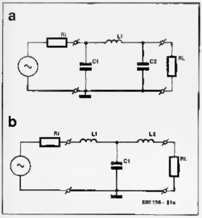


Fig. 12. Passive filters with equal input and output impedances ($R_i = R_L$): (a) π-type; (b) T-type

- One whose input and output terminating impedances are equal (primarily used in h.f. applications). This type of filter is normally constructed in a π- or T-shape as shown in Fig. 12. A number of sections may be simply cascaded to form a C-L-C-L-C or an L-C-L-C-L network. Note that Ri is the internal source resistance.
- One that is connected to a signal source with negligible internal resistance and terminated into an impedance R_L.

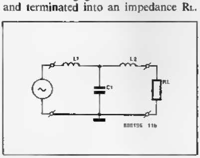


Fig. 13. Passive filter connected to a source of negligible internal resistance and terminated in R_L.

This type, normally constructed in a T-shape (see Fig. 13), is used primarily in low-frequency applications. Several sections may be cascaded to form an L-C-L-C-L network.

For clarity's sake, the sections are shown with an odd number of capacitors and inductors, although an even number is perfectly permissible (for instance, one capacitor and one inductor).

Other combinations of input and output impedance are, in principle, possible, but the two versions described here will suffice for the vast majority of passive filter applications.

The tables, given later in the series, show the component values for each of the two versions at a frequency of 1 Hz. The value of the inductor, L', at the required cut-off frequency is calculated from:

$$L' = LR_L/f \qquad [7]$$

and that of the capacitor, C', from:

$$C' = C/fR_L \qquad [8]$$

Active low-pass sections

Configuration with voltage follower. The simplest form of active low-pass section, shown in Fig. 14, uses an opamp connected as voltage follower. Amplification in the pass-band is unity. This type of filter should be driven from a signal source with very low internal impedance. The output impedance of the filter is also very low. Fig. 14a shows a two-pole version (one pair of conjugate poles), whereas Fig. 14b illustrates a three-pole type (one pair of conjugate poles and one real pole). The three-pole version can be used only in odd-order layouts in view of its single real pole.

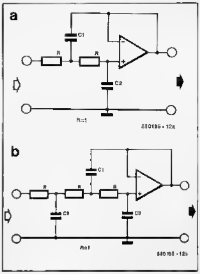


Fig. 14. Active filter with opamp connected as voltage follower: (a) two-pole type and (b) three-pole version.

Depending on the required function, a number of these sections may be cascaded. For instance, for a sixth-order filter three two-pole sections need to be connected in series; for a fifth-order network, a two-pole section is connected in series with a three-pole version. A function requiring an odd number of poles may also be realized with a number of two-pole types followed by a passive *RC*

network as shown in Fig. 15a. If the input impedance of the circuit connected to the filter output is so high that it may be ignored, a buffer terminating the *RC* network is not needed. In other cases the circuit of Fig. 15b may be used, in which the amplification of the opamp may be set with the aid of resistances R_A and R_B (amplification $A = 1 + R_A/R_B$).

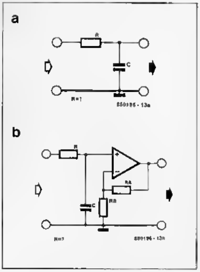


Fig. 15. A real pole may be obtained from a simple *RC* network (a). The addition of an opamp (b) enables buffering and amplification.

The transfer function of the two-pole filter in Fig. 14a is:

$$T(j\omega) = 1/[C_1C_2(j\omega)^2 + 2C_2(j\omega) + 1] \quad [9]$$

in which all resistors have been given a value of 1. The value of the two capacitors as a function of the real and imaginary part of the complex pair of poles may be computed from:

$$C_1 = 1/2\pi\alpha \quad [10]$$

$$C_2 = \alpha/2\pi(\alpha^2+\beta^2) \quad [11]$$

The transfer function of the three-pole network in Fig. 14b is:

$$T(j\omega) = 1/[C_1C_2C_3(j\omega)^3 + 2C_3(C_1+C_2)(j\omega^2) + (C_2+3C_3)(j\omega)+1] \quad [12]$$

In this equation, the values of the capacitors can not be given simply as a function of α and β. Their computation really needs to be done with the aid of a computer.

In a network with one real pole, the value of the capacitor is given by:

$$C = 1/2\pi\alpha \quad [13]$$

The values of the capacitors in two- and three-pole filters with a voltage follower are calculated from the tables ($f = 1$ Hz!) at the required cut-off frequencies. This is done by choosing a value for *R* and determining the required cut-off frequency and then calculating *C'* from

$$C' = C/fR \quad [14]$$

When two or more sections are cascaded, the value of *R* need not be the same for each section, but that of the frequency must, of course, remain the same throughout.

If a number of two-pole sections is to be combined with a section with one real pole (Fig. 15a or Fig. 15b) to obtain an odd-order filter, bear in mind that the tables give capacitor values for the last two-pole section and the passive section that are different from those given for the three-pole filter.

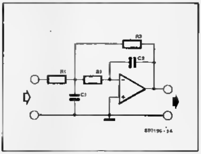


Fig. 16. A two-pole filter with adjustable amplification.

Two-pole filter with amplification. The two-pole section in Fig. 16 offers variable (preset) amplification. The various components are calculated from:

$$C_1 = (A+1)(1+\beta^2/\alpha^2) \quad [15]$$

$$C_2 = 1$$

$$R_1 = \alpha/2\pi A(\alpha^2+\beta^2) \quad [16]$$

$$R_2 = (AR_1)/(A+1) \quad [17]$$

$$R_3 = AR_1 \quad [18]$$

The computation is usually started by giving an arbitrary (standard) value to C_2 and then calculating the other components from the given formulas.

This type of filter, if desired, may be combined with the other filters described earlier. It is, for instance, possible to create a sixth-order network from two sections as shown in Fig. 14a and one as illustrated in Fig. 16.

State-variable filter. In some applications, the state-variable filter offers definite advantages over the filters described so far. The poles and zeros of this type of filter can be arranged fairly accurately, which in other types is next to impossible owing to the effect the components have on one another. Moreover, the bandwidth and amplification of the opamp have little effect on the filter characteristics. This type of

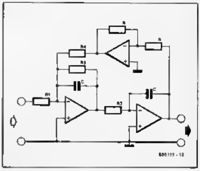


Fig. 17. The state-variable filter is used mainly in applications where the poles and zeros must be arranged fairly accurately.

filter can have some degree of amplification.

The various components are calculated from the following formulas:

$$R_1 = 1/[2\pi AC\sqrt{(\alpha^2+\beta^2)}] \quad [19]$$

$$R_2 = 1/4\pi\alpha C \quad [20]$$

$$R_3 = 1/2\pi C\sqrt{(\alpha^2+\beta^2)} \quad [21]$$

$$R_4 = R_3 \quad [22]$$

If the amplification is unity, $R_1 = R_3$.

Here again, the calculation is started by giving *C* an arbitrary (standard) value, after which the other components can be computed

To finalize the design, the resonance frequency, f_o, and the Q-factor of the filter are calculated for a real cut-off frequency, *f*, from:

$$f_o = f\sqrt{(\alpha^2+\beta^2)} \quad [23]$$

$$Q = f_o/2f\alpha \quad [24]$$

The value of R_3 is adjusted to give maximum voltage at the band-pass output of the filter (output of A_1) when a signal of frequency f_o is applied to the input.

Also at the output of A_1, the bandwidth is measured and R_1 adjusted until this corresponds with that taken for the calculation of the Q-factor ($B = f_o/Q$).

It is clear that in the case of a state-variable filter it is advisable to make R_1 and R_3 a series combination of a fixed and a multi-turn preset potentiometer.

Next month's instalment will deal with high-pass sections and their computations.

EPROM-CONTROLLED TIME SWITCH

by J. Vinckier

Time switches can take many shapes. Where apparatus has to be switched on and off at regular intervals, a simple electronic switch will suffice. This article describes such a device that is controlled by a suitably programmed EPROM. It has battery back-up to ensure continued operation in the case of mains failure.

The circuit consists essentially of three parts: a crystal-controlled time base, IC1 and IC2; an address counter, IC4; and an EPROM, IC3.

The time basis is controlled by a 32.768 MHz crystal, X1, which is of a type frequently used in quartz watches and clocks. The 14-stage counter on board IC1 divides the oscillator signal to 2 Hz. That signal is fed to a second counter, IC2, whose Q6 output is connected to address counter IC4. The frequency of the signal at Q6 is 1/64 Hz: the address counter therefore receives a pulse every 64 seconds, upon which it increases its content by 1.

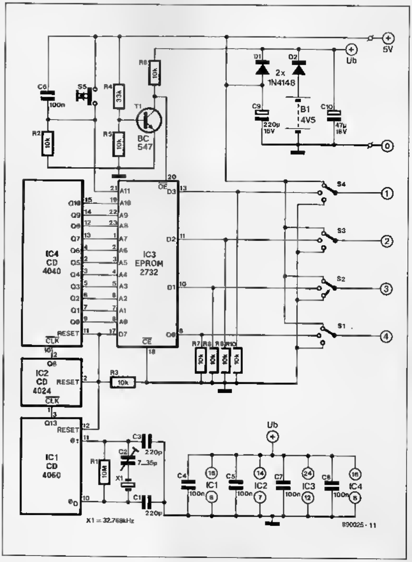
The QØ—Q10 outputs of the address counter are connected to address lines AØ—A10 of the Type 2732 EPROM. After 1,350 clock pulses, that is, 24 hours, the address counter must be reset to Ø. For that purpose, data output D7 of IC3 is connected to the reset inputs of IC1, IC2 and IC3. At address 1350 in the EPROM, a logic 1 is programmed at bit position 7, so that when this counter position is reached, all counters are reset to Ø.

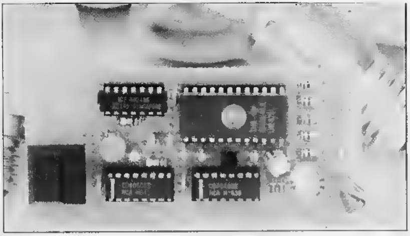
Data lines DØ—D3 of the EPROM are used as control outputs, so that up to four different apparatuses may be controlled, each at the same or different times. Depending on the data at memory positions Ø—1349 in IC3, these outputs are logic Ø or logic 1.

To enable manual control of the apparatuses, each output is provided with a three-position switch, S1—S4. The switches make it possible for an apparatus to be switched on, switched off, or to be connected to the time switch. The on and off switching may also be done with the aid of relays or electronic switches (optocoupler with triac). In the latter case, take great care to ensure good electrical isolation and a safe construction.

The supply for the switch may be obtained from a mains power supply with possibly a 5-V regulator. In case of mains failure, there is a 4.5-V back-up battery, B1. In that condition, only the four ICs remain powered to ensure the continued running of the clock. However, T1 disconnects the outputs of the EPROM to limit the total current drawn to a minimum. During normal mains operation, T1 is switched on via the +5 V line, which causes the $\overline{OE}$ input of IC3 to go low, so that the data are present at the EPROM outputs. During mains failure, T1 is switched off and the $\overline{OE}$ input is high.

Spring-loaded switch S5 is provided to reset the time switch manually at any





Time	RT	Address	D7	D6	D5	D4	D3	D2	D1	D0	Data (hex)
0800	0000	0	0	0	0	0	1	0	1	0	0A
0900	0100	56	0	0	0	0	1	0	1	1	0B
1000	0200	113	0	0	0	0	1	0	0	1	09
1830	1030	591	0	0	0	0	0	1	0	1	05
1930	1130	647	0	0	0	0	1	1	0	1	0D
2000	1200	675	0	0	0	0	1	1	1	1	0F
2030	1230	703	0	0	0	0	1	0	1	1	0B
2100	1300	731	0	0	0	0	1	0	1	0	0A
2200	1400	788	0	0	0	0	1	0	0	0	08

0759	2359	1349	0	0	0	0	1	0	0	0	08
0800	0000	1350	1	0	0	0	1	0	0	0	78

		4095	1	0	0	0	1	0	0	0	78

given time: this has to be borne in mind during the programming. It is thus, for instance, possible to arrange the programming to start at 8 o'clock in the morning. Reset switch S5 is then pressed at 8 o'clock next morning and from then on the programming will ensure that all instructions are carried out correctly.

Construction and programming

The circuit may be constructed on a piece of prototyping or vero board. Even the batteries and switches may be mounted on this board. It is, however, strongly advised to fit the mains-carrying parts, including any relays (mechanical or electronic) on a separate board. Note, however, that a prototyping board is not safe for this purpose. The low-voltage and mains-carrying parts may be mounted on the same board if they are electrically well separated by the removal of some tracks and solder pads between the two sections.

Programming

It is possible to calculate the switching times by hand and a simple calculator. For example,

- start time (address Ø) - 0800 h;
- output 1: on 0900 h, off 2100 h;
- output 2: on 2000 h, off 2200 h;
- output 3: on 1830 h, off 2030 h;
- output 4: off 1830 h, on 1930 h.

First tabulate the relative times, that is, the periods between the start time and the switching times. The EPROM address is then computed by converting the relative time (RT in the table) into seconds and divide the result by 64. The examples above are worked out in the table. Note that the memory positions between two addresses must be filled in with the last stated data, for instance, the addresses 1 to 55 must be given the same data as those for address 0. It should be borne in mind that all addresses from 1350 onwards must have a 1 at data bit 7 to ensure that the reset function operates correctly.

NEW PRODUCTS

Accelerometer

THE VII accelerometers from Shinken Co. of Japan are piezoelectric transducers which convert mechanical movements into electrical signals proportional to the acceleration. The accelerometers feature rigid construction wide frequency range and high linearity and are used in conjunction with any digital vibration meter and charge amplifier. Nine models are available in this series. The charge sensitivity is from 45 pc/G to 26 pc/G. Voltage sensitivity is from 50 mV/G to 20 mV/G. The maximum acceleration these units can withstand is from 100 G to 1000 G. The temperature ranges from 70°C to 250°C.

M/s. Murugappa Electronics Ltd. • Agency Division • 29, Kamraj Avenue Second Street • Adayar • Madras-600 020 • Phone 41 33 87.

Digital PH Meter

The Naina solid-state digital pH meter features electrode socket and in-built voltage stabiliser. The continuous range extends from 0 to 14 pH and 0 to ± 1999 mV with relative accuracy of ± 0.01 pH and ± mV. Options include : recorder output, automatic temperature compensation, temperature indication and slope correction.

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DEALING WITH ELECTROMAGNETIC INTERFERENCE

by Alan Baker, BSc(Eng), ACGI, CEng, FIMechE

Electromagnetic interference (EMI), almost ignored about ten years ago, has now become important, primarily because of the proliferation of electronic equipment in aerospace, motor vehicles and other industries.

A feature of such equipment is its sensitivity to electromagnetic emanations in the environment, and it cannot be completely shielded from them. Consequently there is widespread interest in assessing the levels of EMI likely to be encountered in various circumstances and in developing valid methods of testing the susceptibility of different types of electronic systems.

Laboratories devoted to these activities have therefore sprung up worldwide, some for particular industries and others in university engineering departments. The latest, for the automotive industry, is the electromagnetic compatibility (EMC) laboratory officially opened last year for the Motor Industry Research Association (MIRA) at Nuneaton.

This is especially timely in view of the rapid growth of vehicular electronic applications such as ignition systems, engine and transmission management, adaptive and active suspensions, antilock brakes and four-wheel steering. The effect of any malfunction caused by EMI on these items can range from simple annoyance to a catastrophe.

Europe's largest laboratory

MIRA's EMC department is not yet six years old but its early growth rate was so rapid that the need for expansion was already obvious to its then director, Dr Cedric Ashley, before the end of 1984. He subsequently gained financial support from Britain's Department of Trade and Industry, the Department of Transport, the Metropolitan Police in London, and seven companies (Eaton, Ford, Jaguar, Lotus, Lucas, SPA and Saab Scania).

With MIRA's £500 000 contribution there was enough money to do the job properly, resulting in Europe's largest laboratory devoted to this particular sector of automotive technology. The EMC laboratory now has contracts from firms in continental Europe, the United States and the Far East.

Pride of place in the laboratory goes to a large anechoic chamber made of steel and measuring 22 m long × 10 m wide × 7 m high. This is big enough to take the maximum weight of 38 tonnes for articulated trucks, buses or coaches as well as cars. Most vehicles for testing are of course cars but the sizes are useful for them too as accuracy of measurement is impaired if the walls are too close to the source of emissions.

In the interest of repeatability over a broad range of radio frequencies, the chamber walls and ceiling are lined with energy absorbing pyramids which are 1.8 m long and made of polyurethane foam impregnated with carbon.

Regenerative braking system

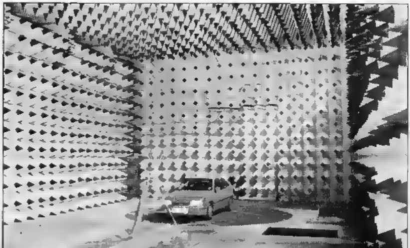
On the floor of the chamber are two sets of vehicle-driven aluminium rolls and a turntable. The rolls drive a large two-axle electric dynamometer installation with a continuous absorption capacity of 150 kW per axle — an input that demands a highly efficient cooling system.

The diameter of the rolls is unusually large at 1.5 m to keep tyre temperature down to acceptable levels, and their maximum peripheral speed is 160 km/h. One of the axles is fixed while the other can be moved to give any desired wheelbase between 2 m and 6.5 m.

The dynamometer operating modes include road load, wheel slip and antilock braking — the latter with decelerations as high as 2 G. A lot of energy has to be dissipated on continuous cycling tests, despite the relatively low mass of the rolls, so the dynamometer incorporates a regenerative braking system.

Braking can be applied to both axles but it is not normally used on the driving one because of possible tyre-rating problems.

The dynamometer, made by Brush Electrical Machinery of Loughborough, enables a wide selection of vehicles to be driven as though on the road while being



The interior of the anechoic chamber which is big enough to take trucks and buses as well as cars. In the foreground are the two sets of 1.5 m diameter dynamometer rolls and beyond them is the turntable with a capacity of 10 tonnes.

subjected to a full spectrum of electromagnetic radiations.
The turntable, also supplied by Brush Electrical Machinery, has a diameter of 6 m and a load capacity of 10 tonnes and is used for static investigations, particularly of vehicle field coupling which can be fully measured. Bulk current absorption spectra obtained on this equipment can be used for — among other purposes — predicting worst case antenna positions for susceptibility tests on the dynamometer, thus saving quite a lot of valuable time.

Other facilities

Alongside the main chamber are the control rooms equipped for both manual and computer controls. MIRA's specialists reckon that this combination of equipment and control systems gives them full competence to evaluate the EMC performance of most common types of vehicle in repeatable and realistic operating conditions over a frequency range from 10 kHz to 1 GHz and with field strengths of up to 200 V/m at 1 m distance.
Outside the laboratory building is a site for measuring whole vehicle radio frequency emissions in actual field conditions to meet statutory requirements. There are also indoor facilities for assessing the susceptibility of electronic sub-systems.
One of these facilities is for bulk current injection, carried out by clamping on electrodes and thereby inducing high frequency currents in the wiring loom, on or off the vehicle, so that their effects on the electrical equipment can be studied. A highly adaptable routine has been developed whereby the testing can take in a single conductor, a group of them or the entire harness.
The susceptibility of electronic equipment to transverse electromagnetic mode (TEM) radiation can be measured on a standard stripline over a frequency range from 10 kHz to 400 MHz at field strengths over 20 V/m. For small objects this apparatus is complemented by a TEM cell with a lower maximum frequency but the capability for considerably higher field strengths of up to 1000 V/m.
Last of the laboratory's facilities is a relatively small non-anechoic screened chamber measuring 5 m long × 3 m wide × 2.3 m high. It is used for giving radiated susceptibility and emission tests to components and sub-systems by the special techniques defined in various European and United States military standards.
Generally, therefore, the MIRA laboratory does not only offer a capability test but provides the world's motor industry with a problem-solving service, ranging from the evaluation of circuit design and the rectification of faults to the complete design of equipment and its final electromagnetic compatibility testing.

ELECTRONICS NEWS

Plan Outlay

The Planning Commission has approved Rs. 2,725 crores for the telecom sector for 1989-90. The commission has been soft on telecom for it effected only a marginal cut on the projected demand of Rs. 2,775 crores.

The DOT is expected to meet 75 per cent of its expenditure through internal resources. The budgetary support is only about Rs. 225 crores. the department has sought to raise an additional Rs. 300 crores by issuing bonds and the Planning Commission has supported the DOT's plea.

The 1989-90 plan envisages commissioning of five lakh new phone connections against the four lakhs for 1988-89. Against 69 cities connected by STD in 1988-89, next year 113 cities will come under the STD network.

Indo-Soviet PC

The Soviet Union is seeking Indian technology for the manufacture of LBM compatible personal computers. It has agreed to set up a joint venture with India for the manufacture of these computers.

The Soviet Union may buy back 100,000 computers annually from the proposed unit. There is a large demand for PCs in the Soviet Union which are manufactured on a big scale. However, the Soviet Union is keen on switching over to the IBM compatible because of their universal acceptability.

The decision to set up a joint venture unit for the small computers was taken at a meeting of the Indo-Soviet working group on electronics and computers. The working group also envisaged collaboration in other fields including manufacture of electronics components and software. The Soviet Union is keen on exporting ICs to India. It has agreed to undertake an agressive marketing drive popularise the Soviet made ICs. In the next few months, the Soviet Union will hold a series of seminars in India relating to the ICs.

VCR-VCP Technology

India is exploring the possibility of obtaining the technology for VCR-VCP manufacture in the country through small Japanese companies.

Japanese multinationals have been advised not to transfer the "head drum" technology to any country and even the sale of VCRs in CKD conditions is being stopped. However, small component manufacturers, who are the captive suppliers of big Japanese firms, are believed to be exempt from this restriction on technology transfer.

In India, the Electronics Trade and Technology Development Corporation (ET & T) has been allowed to have a collaboration with the Tohei of Japan. Tohei is a manufacturer of VCR components, including the tape deck mechanism. In the 1970s, the company supplied the decks for over three million VCRs manufactured by Hitachi. The company will manufacture the tape deck mechanisms for India with a promise of technology transfer, it is reported.

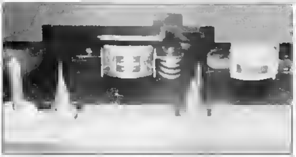
ET & T proposal envisages 25 per cent indigenisation from the very beginning while the other private manfuacturers have agreed to reach 70 per cent indigenisation in five years.

The large Japanese companies are just assemblers of components made by small, captive component manufacturers and these small units possess the technology. Tohei, being a small sector company, can transfer the technology without much difficulty, it is believed. ET & T hopes to reach the international prices of VCRs and VCPs in two or three years.

Tohei is one of the six companies earlier short listed for collaboration. The company has already been having a tie up with the Calcutta firm, Sonodyne-Indian Fine Bank, for making cutting dies and material processing machinery. Sonodyne-IFB will be nominated suppliers for key parts of VCRs and VCPs produced by the ET & T and ECIL, joint venture. The company would be allowed to assemble the VCRs manufactured by ET & T.

RECORDING/PLAYBACK AMPLIFIER

This amplifier enables accompanying slide presentations with stereo commentary or music whilst using a separate track on the cassette recorder for controlling the slide changer.



This simple to build amplifier makes use of a 4-track recording/playback head fitted in lieu of the 2-track head in an ordinary cassette recorder used for audio-visual presentations. Four-track heads can be picked up occasionally from surplus outlets, or purchased as a servicing part for auto-reverse cassette players. The proposed signal assignment on the 4-track head is shown in Fig. 1. The non-used track in between those assigned to the stereo programme and the control signal ensures acceptable levels of crosstalk. The programme and the slide control signal can be recorded separately. If required, the control pulses can be erased by reversing the cassette and recording silence

Circuit description

The circuit diagram in Fig. 2 shows that the recording/playback amplifier is set up around the Type TDA1002A integrated amplifier from Mullard. Although this component is not aimed at the high quality market, its technical qualities are still adequate for use with most types of (semi-portable) stereo cassette recorders or decks commonly available. The TDA1002A requires relatively few external components to make a versatile recording/playback amplifier. As shown in the circuit diagram, the chip comprises a preamplifier and a recording amplifier with automatic level control (ALC). The control range of the ALC circuit is stated as 50 dB ±2 dB.

When 4-pole toggle switch S_1 is set to RECORD as shown in Fig. 2a, the slide control pulses are applied to pin 1 of the TDA1002A via switch section c and terminal C. Also, the RECORD LED lights (section a), and one side of the symmetrical output of the record/playback head is grounded. Since terminal D is connected to E (section d), the preamplifier works with feedback circuit C_4-R_3 connected in series between output pin 4 and input pin 2. The amplified signal is available at the output of the circuit, but it is also fed to the input of the recording amplifier (pin 8) via R_8-C_7, and the input of the ALC circuit (pin 6) via R_6. The input of the recording amplifier is held at a fixed potential with the aid of voltage divider R_{11}-R_{10}-R_9. The negative feedback network between output pin 9 and input pin 7 is composed of R_{12}-R_{15} incl. and C_{11}-C_{14} incl. The ALC circuit acts on the output of the recording amplifier via R_{17}-R_{18}-C_9. The limiting time (10 ms typ) and the recovery time (35 s typ.) are fixed with C_{15} and C_{16}-R_{19} respectively. The amplified and limited recording signal is fed to the head via C_{13}-R_{16}, terminal A, switch section b and R_1.

When S_1 is set to the PLAY mode, terminal A is grounded via switch contact b, LED D_1 is extinguished, and the playback signal from the head is fed to the input of the TDA1002A. Switch section d selects negative feedback network R_5-C_5-R_6 between the output and the input of the preamplifier, which is so dimensioned to give the appropriate gain. Note that the ALC and the recording amplifier are ineffective in the PLAYBACK mode. The output signal can be fed to the available slide change circuit.

The circuit is fed from a regulated 10 V supply set up with IC_2. The unregulated input voltage should not exceed about 15 V. It may be necessary to redimension R_{20} in accordance with the regulated or unregulated voltage available in the cassette recorder.

Construction and setting up

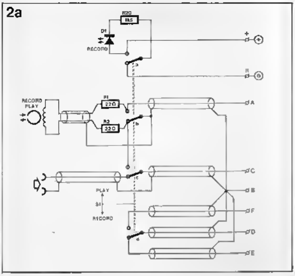
The layout for the printed circuit board for building the recording/playback amplifier is shown in Fig. 3. Note that the board does not hold the parts shown in Fig. 2a. It is recommended to fit the completed PCB at a suitable location in the cassette recorder. Most types of low cost, modern cassette deck have plenty of space inside to house a small additional PCB, and generally do not present problems as regards the supply current for the proposed amplifier. The 4-pole toggle switch, S_1, and the LED, D_1, are fitted on the front panel.

Carefully remove the existing stereo head, and make sure to have connection data of the 4-track head available before this is fitted. In some cases, the new head requires a few modifications to be carried out on the existing head mounting assembly, and possibly to the azimuth adjustments also. Refer to Fig. 1 and connect the two recording/playback channels of the head to the existing circuitry in the recorder. Connect the head section for the slide control signal to R_1-R_2 (these are fitted direct onto S_{1b}) via a short length of shielded, symmetrical wire, grounded centrally at terminal B as shown in Fig. 2a. It should be noted that the equalization characteristics of the TDA1002A are dimensioned for Fe cassettes only. The total gain of the device is about 40 dB at an average distortion of 0.5%. The maximum input and output voltage are 20 mV_{rms} and 2 V_{rms} respectively. The input impedance is about 16 kΩ. Depending on the sensitivity of the head used, the stated value of R_{16} may have to be slightly altered to ensure the amplitude of the recording signal. Resistors R_3 and R_4 determine the gain of the playback amplifier. Low frequency oscillation may occur when the amplifier is dimensioned for a relatively low gain.

Test the newly installed 4-track

1

Fig. 1. Suggested track assignment on a 4-track head.



head by first playing a prerecorded stereo music cassette, or, if available, a test cassette. Adjust the head until the quality of the playback signals is acceptable. Rewind the tape to the start, and replay it while using the recording/playback amplifier for recording the slide control signal on the third track. Stop the tape, rewind it, and check whether all signals are played back at acceptable levels of distortion and crosstalk. Slide change signals of a wide amplitude range can be recorded without causing tape saturation, thanks to the ALC circuit in the recording/playback amplifier. *R*

Parts list

Resistors (±5%):

R_1;R_2 = 22R
R_3 = 6K8
R_4 = 220R
R_5 = 560K
R_6 = 12K
R_7 = 100R
R_8;R_{11} = 33K
R_9 = 100K
R_{10} = 68K
R_{12} = 2K7
R_{13} = 180R
R_{14};R_{15} = 27K
R_{16} = 2K2
R_{17},R_{18} = 10K
R_{19} = 1M0
R_{20} = 1K5

Capacitors:

C_1,C_4;C_8,C_9;C_{10} = 10µ; 16 V; axial
C_2,C_{14} = 3n9
C_3 = 100µ, 16 V; axial
C_5,C_{17} = 10n
C_7 = 100n
C_6 = 47µ; 16 V, axial
C_{11} = 220p
C_{12} = 22µ, 16 V, axial
C_{13} = 15n
C_{15} = 4µ7; 16 V, axial
C_{16} = 220µ; 16 V; axial
C_{18} = 330n
C_{19} = 820p

Semiconductors:

D_1 = red LED
IC_1 = TDA1002A* +
IC_2 = 78L10*

Miscellaneous

S_1 = miniature 4-pole toggle switch.
4 track recording/playback head for cassette recorder

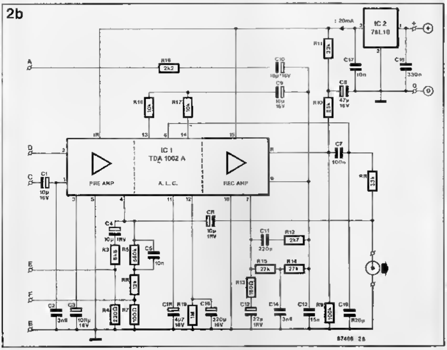


Fig. 2. Circuit diagram of the recording/playback amplifier.

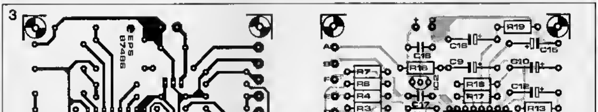


Fig. 3. Track layout and component mounting plan of the PCB for building the recording/playback amplifier.

electronic nuisance

an infuriating

W. Verbiest

Have you ever been kept awake by a cricket? You switch off the light and snuggle down, and just as you're drifting off to sleep the insect starts to make an irritating noise. As soon as you switch on the light to look for it, it stops again. Tracking down this type of noisy nocturnal nuisance can be infuriatingly time-consuming. The same result can be obtained electronically. What's the point? Well, just for the fun of it.

Practical jokers will want to hide the circuit in such a way that it will take some time to find it. For this reason, it must be small; furthermore, it will have to be battery-powered — a mains cable would be a dead give-away. The circuit described here fulfils both requirements it fits on a small p.c. board and is powered by a small 9 V battery

The light sensor is an LDR. In the dark, its resistance is quite high; preset potentiometer P1 is adjusted so that the inputs of the CMOS gate N1 are just at logic zero under these conditions. The calibration procedure will be described later.

The two CMOS gates, N1 and N2, are connected as a 'trigger' circuit. When the voltage at the inputs of N1 falls below the trigger threshold, the output of N2 switches to logic zero Transistor T1 is turned off, and C1 can now charge up through R5.

The voltage across C1 rises so slowly that it takes a few minutes for it to reach the upper trigger threshold of the second trigger circuit, N3 and N4. At that point, the output of N4 swings up to logic one — i.e. practically the full supply voltage This takes the reset input of the 555 timer (IC2) high, enabling this IC. The 555 is used in an oscillator circuit, driving a loudspeaker, so that an irritating tone is produced.

When the victim turns on the light to hunt for the source of the noise, the resistance of the LDR decreases sharply. The trigger circuit (N1/N2) changes state, turning on T1, C1 discharges rapidly through R4, the output of the second trigger circuit goes 'low' and the oscillator is turned off.

When the light is switched off again, the circuit again waits a few minutes before making a noise. Very infuriating . . .

Calibration

Preset potentiometer P1 must be adjusted so that the inputs of N1 are at logic zero when the circuit is in the dark The easiest way to do this is to connect a voltmeter to the output of N2 First, P1 is adjusted so that this output swings up to nearly full supply

voltage, then P1 is turned back until the output switches to the 'low' level (practically 0 V) — with the LDR in the dark, of course. This completes the calibration.

The time delay, from the moment the light is turned off to the first squeak from the oscillator, can be modified according to personal taste by altering the value of C1. In the same way, a different frequency can be obtained by selecting a different value for C2. The ratio of resistor R9 to R10 determines the type of sound obtained.

Finally, the sound level depends on R8. Note, however, that this resistor should not be less than 100 Ω. Any loudspeaker impedance from 4 Ω up can be used; the higher the impedance, the louder the output. ■

1

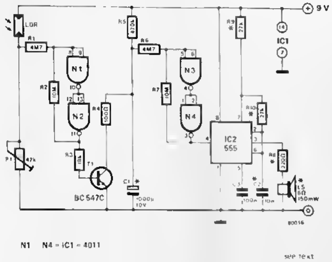


Figure 1. Not much is needed for an electronic nuisance. The LDR turns the circuit on in the dark.

2

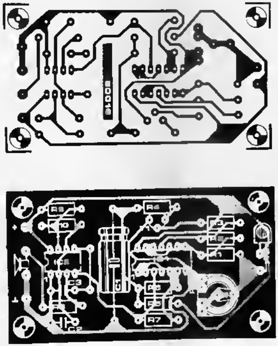


Figure 2. All the components for the nocturnal nuisance fit on this p.c. board.

Parts list

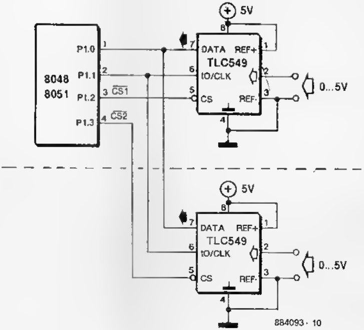
Resistors
R1,R6 = 4M7
R2,R7 = 10 M
R3 = 10 k
R4 = 100 Ω
R5 = 470 k
R8* = 220 Ω
R9*,R10* = 27 k
P1 = 47 k preset potentiometer
LDR

Capacitors
C1* = 1000 µ/10 V
C2* = 10 n
C3 = 100 n

Semiconductors
T1 = BC 107B, BC 547C or equ.
IC1 = 4011
IC2 = 555

* see text

SMALL 8 BIT A-TO-D CONVERTER



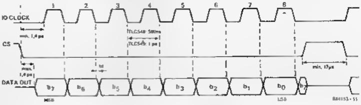
The TLC548 and TLC549 from Texas Instruments are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor. A conversion can be completed in 17 µs or less, while complete input-conversion-output cycles can be repeated in 22 µs for the TLC548 and in 25 µs for the TLC549.

The internal system clock and I/O clock are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the 'conversion crunching' circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the data output pin is in a high-impedance condition and the I/O clock pin is disabled. This $\overline{CS}$ control function allows the I/O Clock pin to share the same control logic point with its counterpart pin when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and the a falling edge of the internal system clock after a $\overline{CS}$↓ before the transition is recognized. However, upon a $\overline{CS}$ rising edge, DATA OUT will go to a high-impedance state within the t_{dis} specification even though the rest of the IC's circuitry will not recognize the transition until the $t_{su(CS)}$ specification has lapsed. This technique is used to protect the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result will initially appear on the DATA OUT pin when $\overline{CS}$ goes low.



2. The falling edges of the first four I/O clock cycles shift out the 2nd, 3rd, 4th and 8th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th high-to-low transition of the I/O Clock. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.

3. Three more I/O clock cycles are the applied to the I/O pin and the 6th,7th and 8th conversion bits are shifted out on the falling edges of these clock cycles.

4. The final, (the 8th), clock cycle is applied to the I/O clock pin. The on-chip sample-and-hold begins the hold function upon the high-to-low transition of this clock cycle. The hold function will continue for the next four internal clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. $\overline{CS}$ can be kept

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

For certain applications, it is necessary to start conversion at a specific time. This is achieved by stopping the I/O clock after the leading edge of the 8th pulse. Conversion is started by making the I/O clock low at the desired time. During the period when the I/O clock is high, the sample-and-hold will continue to sample the analogue input

low during periods of multiple conversion. When keeping CS low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O Clock line. If glitches occur on the I/O Clock line, the I/O sequence between the microprocessor/controller and the device will lose synchronization. If CS is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of CS will cause a reset condition, which will terminate the conversion in progress.

The circuit shows how two converters may be connected to a Type 8051 or Type 8048 controller. It is, however, also possible to connect fewer or more than two converters.

The program shown is a test aid for converters connected to a Type 8051. If the ports of the 8051 shown are already occupied, or if something else has been connected to the other lines of port 1, the program must be suitably altered (the highest bits of P1 must be logic high).

```
10 REM COMPUBOARD TEST PROGRAM FOR 8 BIT AD-CONVERTER TLC548/549
20 REM
30 PORT1 = 0FDH:                                REM CS = 1, clock = 0

40 REM *********** MAINLOOP *************
50 DO:                                          REM do forever
60  GOSUB 1000
70  PRINT "AD-value = ",
80  PRINT USING(###), VALUE, CR,
90 UNTIL 0
100 END

1000 REM READ CONVERTER
1010  PORT1 = 0F9H:                             REM CS = 0, clock = 0
1020  VALUE = 0
1030  FOR BITCNT = 0 to 7
1040   VALUE = (VALUE*2).OR.(PORT1.AND.01H):    REM shift in new bit
1050   PORT1 = 0FBH: PORT1 = 0F9H:              REM clock pulse
1060  NEXT BITCNT
1070  PORT1 = 0FDH:                             REM CS = 1, clock = 0
1080 RETURN
```

884093 - 12

The supply voltage is used as the reference voltage, which obviates the use of external components. The differential reference input does, however, offer full freedom in choosing a different reference voltage.

The total conversion error introdu by the converter is ±0.5 LSB w U_{ref} = 5 V.
The current drawn by the IC is 3 max.

CALSOD, A LOUDSPEAKER DESIGN PACKAGE

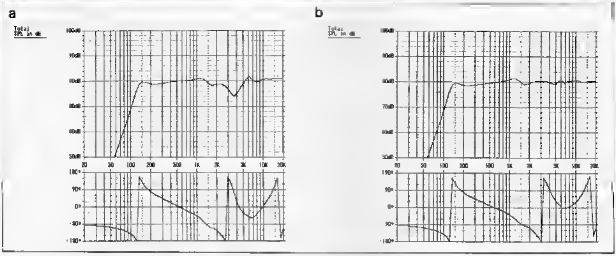
Until recently, computer-aided loudspeaker design and optimizing could only be implemented on mainframes. Fortunately, that has changed, and a new, comprehensive, design package, CALSOD, is now available for PCs as well. This article reviews CALSOD, and reports on its use in a practical test.

Designing a good-quality loudspeaker box invariably requires solid background knowledge, a lot of time, and reliable test equipment. If any one of these three ingredients is lacking, the final design will almost certainly fail to give satisfactory results. Serious designers will no doubt have the relevant equipment and background knowledge, but often lack time to go through the stages of testing and redesigning the box. The design of a multi-way loudspeaker system invariably commences with setting up a theoretical model on the basis of available data on the drive units to be used. Next, a prototype is built to clear the way for practical tests. Measurement results generally deviate widely from those expected on the basis of the calculations. This is so because it is very hard, if not impossible, to include each and every parameter in the calculations. Filter response, impedance, frequency and phase characteristics of the drive units are all fairly simple to determine on their own, but complex calculations in simulation programs are required to predict their combined effect, leading up to the total response of the filter and drive units. Unfortunately, the development and use of such simulation programs is the exclusive domain of leading loudspeaker manufacturers. Not only the software investment, but also the mainframes used for running these programs are well out of reach of individual box designers and small companies. The arrival of CALSOD has changed this radically. Other software packages for loudspeaker design and optimizing, offering a price/performance trade-off at least equal to that of CALSOD, are, to the best of our knowledge, not available.

Computer-aided design

CALSOD stands for Computer-Aided LoudSpeaker Optimizing and Design. Although 'Design' would normally precede 'Optimizing', the acronym covers the function of the package very well. A series of extensive tests with CALSOD has spurred our enthusiasm about the program. The redesign feature of the program was tested on existing loudspeaker systems. Remarkably, CALSOD's computed response was found to correspond exactly with the measured response.

CALSOD is actually a set of sub-programs that together offer the possibilty to calculate everything a designer needs to know to achieve optimum results from the available drive units, whose technical characteristics are first entered in the program (impedance, frequency and phase response; Thiele/Small parameters, if available). Obviously, accuracy of the computed results is determined to a large extent by the accuracy of the input data. A number of fairly simple program modules then allow converting the measured curves into a kind of equation used for processing by the program. Examples of available filter modules include one capable of generating a second to fifth-order Butterworth characteristic, one representing the response of a drive unit in a closed box, a bass reflex box, a passive radiator, and so on. Small irregularities in a response curve can be simulated accurately with the aid of so-called 'minimum phase equalizers', which are essentially tuned circuits whose resonance frequency, Q (quality-)



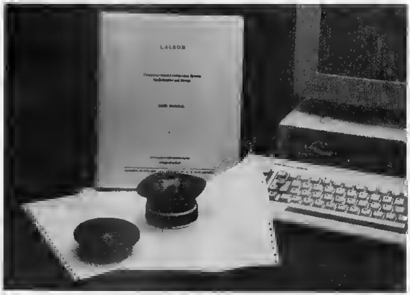
These graphs show the total acoustic output of a two-way loudspeaker system before (a) and after (b) optimizing with CALSOD.

factor, and amplification or attenuation can be specified by the user.

After the curves have been simulated with the aid of modules, these can be 'fitted with' the appropriate filters. All data is put into a text file that looks similar to a netlist for SPICE. The integrated word processor is then used for making a file for each loudspeaker. The file contains the component values, and the way components are connected to nodes in the network. Global values can be entered for filter specifications, e.g., representing an ideal filter terminated in a pure resistance.

Next, the target response curve is specified, e.g., that of a fourth-order Linkwitz filter dimensioned for a cut-off frequency of 5 kHz. The file with all data is then read into the program, after which network analysis is performed. The user is then in a position to study all the relevant parameters: frequency and impedance characteristics of the box, output voltage of the filter, input impedance of the loudspeaker(s) plus filter, and the acoustic output signal of the box plus filter. The target response curve can be projected over the measured response, so that deviations can be assessed before the optimizing process commences. CALSOD changes component values in the filter until the acoustic output signal is a reasonable approximation of the target specification. The user is in a position to state beforehand which components may be redimensioned by the program. All loudspeaker sections are processed in this way to obtain a larger file that contains optimized data for all sections.

The complete system is then ready for analyzing. Individual curves can be displayed separately, as well as the sum signal produced by the loudspeakers, measured at a predefined distance from the box. CALSOD even offers the possibility to indicate vertical and horizontal position of the loudspeakers on the front



panel of the box, as well as inter-loudspeaker distance relative to the listening position. This facility allows studying the effect of, say, a 3 cm displacement of the tweeter, or a 10 cm displacement of the listener. Finally, CALSOD is a capable of optimizing the complete system, working effectively towards the realization of the target response.

Practical and with plenty of options

CALSOD is a well-designed and remarkably practical program that will prove invaluable to the designer who knows what he is doing. Evidently, the program is and remains but a tool that works on the basis of the user's experience gathered from previous loudspeaker designs. None the less, this tool greatly simplifies formerly often tedious and time-consuming work. The optimizing procedure can provide really good results, and the options for analysing a complete system are unique. On a less positive note, the program is fairly cumbersome to work with. As in SPICE, changing a single value in the input file is basically simple, but time-consuming. Before a new analysis can be performed, the user must return to the word processor, change the text where appropriate, load the modified file into CALSOD, and restart the analysis. Remarkable in view of the fairly heavy calculation load, the review package of CALSOD did not support the use of a maths co-processor in the PC.

"BATTERY LOW" INDICATOR

by J. Ruffell

Today there are innumerable pieces of equipment that are powered by batteries, both dry and rechargeable. In many cases, it is difficult to determine whether those batteries are still fresh or fully charged or if they need replacing or recharging. Here is a small circuit that monitors the battery voltage and gives an audible warning when that voltage becomes too low.

The indicator described here is small enough to enable it being fitted inside the battery-operated equipment, such as a portable shaver or receiver. It draws a current of not more than 1 mA, so that it does not noticeably increase the load on the battery.

Circuit description

The circuit is based on two opamps that are housed in Type TLC272 chip. Opamp A1, connected as a comparator, compares the battery voltage, applied to the inverting input via potential divider R1-(R3+P1), with a reference voltage of about 4.7 V that is applied to the non-inverting input. Owing to the low zener current, the reference voltage is not always exactly 4.7 V. However, when the battery voltage drops, the potential at the inverting input decreases much more rapidly than that at the non-inverting one, so that the comparator always toggles at the same battery voltage. That voltage may be set very accurately by P1. When the battery voltage is at a normal level, the potential at the inverting input of A1 exceeds the zener voltage. The output of the comparator is then virtually nought. When the zener voltage exceeds the voltage across R3+P1, the comparator toggles, which causes the level at its output to rise to that of the battery voltage. Capacitor C2 is then charged slowly via R5. The potential across the capacitor (at the inverting input of comparator A2) is compared by opamp A2 with the voltage at its non-inverting input. Because of the feedback via R7, that voltage does not have a fixed value, but that does not matter in this circuit. When the potential across C2 has attained a value that is higher than that of the voltage at the non-inverting input of A2, the output of this opamp goes low. Darlington T1, and consequently buzzer Bz1, is then switched on. The buzzer is a d.c. type with built-in oscillator. In this condition, the potential at the non-inverting input of A2 is pulled down a few volts via R7; in other words, there is a degree of hysteresis. Because of that, the buzzer will continue to draw current from C2 until the potential across the capacitor (and thus at the inverting input of A2) has decreased by a few volts. The comparator then toggles so that its output goes high, which renders the buzzer inactive. From then on C2 charges again and the process repeats itself until the quipment is switched off and the battery is replaced or recharged.

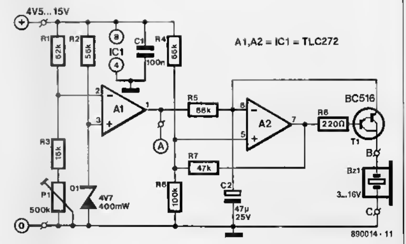
The indicator is suitable for use with battery voltages between 4.5 V and 15 V. When a Type TLC272 IC is used, the circuit draws just under 1 mA. Use of a Type TLC27L2 reduces this to 250 μA at 9 V.

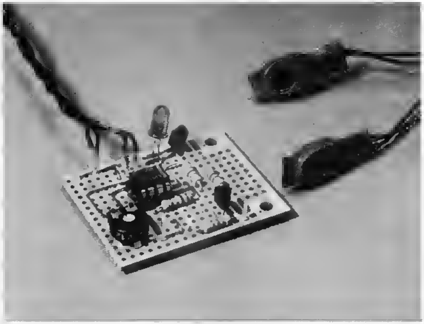
Construction

Since the whole circuit consists of only 15 components, it is easily constructed on a small piece of prototype or vero board. The shape of this should be adapted to the space available in whatever equipment the indicator is to be used.

The circuit is preset as follows. Assuming that the battery voltage is 9 V, the buzzer should start operating at about 7 V. Connect a regulated, variable power supply to the circuit and set its output to precisely 7 V. Turn P1 to maximum resistance. With a multimeter, measure the voltage at the output of A1 (test point A): this should be virtually nought. Slowly turn P1 until the output voltage of A1 suddenly rises to 7 V: this is the correct setting of P1. Within a few seconds, the buzzer should sound.

The indicator can then be fitted into the relevant equipment. Its battery connections should be soldered to suitable take-off points behind the on-off switch.





This photograph shows our prototype of the 'computer eye' and, in the background, the LDRs fitted in shrink sleeves.

To put your mind at rest: the title does not imply that the circuit described here enables a computer to see. But if you want to use your computer for controlling external equipment without connecting this direct to the computer, the proposed circuit will 'keep an eye' on certain output signals of the computer and on that basis switch the equipment on and off. In other words, it provides an optical coupling between the computer and the equipment to be controlled. This does imply, of course, that a monitor screen is available and that the computer has some graphics facilities. Otherwise there would not be much to see for the eye!

computer eye

control by monitor screen

The circuit is based on an opto-electronic comparator as shown in figure 1. The 'eye' proper is formed by two light-dependent resistors — LDRs — R1 and R2. The voltage level at their junction is applied to the inverting input of the comparator, IC1, via R4. The non-inverting input of IC1 is held at a fixed reference voltage. The comparator toggles when the level at its pin 2 is lower than the reference voltage. Transistor T1 is then on, and the relay is actuated. At the same time, T2 conducts, so that the LED, D1, lights to indicate the state of the circuit visually.

When the level at the inverting input of the comparator is higher than the reference voltage, the relay is not energized, and D1 is out.

The idea is that the control program includes instructions which cause two light areas to appear on the monitor screen as required. The intensity of one of these areas should be constant, while that of the second should be either low or high (dark or light). The preferred mode of operation is for the second area to be dark when the external equipment should be switched on, and bright when it is to be switched off.

The LDRs should be attached to the monitor screen where the two light areas appear. The voltage (about 2 V_{pp}) at the junction of these resistors is a measure of the difference in brightness between the two light areas on the screen. Superimposed on this voltage is, of course, the sawtooth voltage produced by the 50 Hz line scan oscillator. Resistor R4 and capacitor C1, and to some extent P1, ensure that this sawtooth voltage does not

1

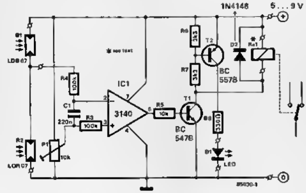


Figure 1. If you do not want to connect all kinds of equipment to your computer, you can still operate that equipment with this 'computer eye': an optocoupler which is nothing but a light-dependent comparator.

affect the correct operation of the comparator.

Construction of the circuit is not critical: all components, except the LDRs, are fitted on a small prototyping board. The LDRs are connected to this board by sufficiently long pieces of stranded equipment wire. It is recommended to fit them in suitable shrink sleeves or swathe them in insulating tape in such a way that only the light of the two areas on the screen falls onto them (see photograph). They can be attached to the screen with some self-adhesive tape. If the equipment to be controlled is switched on when it should be switched off, and vice versa, simply interchange the LDRs.

Presetting of the comparator is not critical as long as the change-over frequency of the two light areas is of the order of 1 Hz. In that case, P1 is simply set so that the relay is actuated and de-energized in rhythm with the change-over frequency. When that frequency is higher, e.g. when the circuit is used for data transfer, the presetting of P1 becomes more critical. The maximum allowable change-over frequency depends on the cut-off frequency of the low-pass filter, R4/C1, which here is less than 10 Hz. Optimum setting of P1 is then best achieved by applying a square-wave voltage at a frequency of about 8 Hz to the comparator input. Measure the output at pin 6 with an analogue voltmeter (10 V d.c. range) and adjust P1 so that this level is half the value of the supply voltage. Although the pointer of the voltmeter quivers somewhat, the setting can be carried out without any trouble. If you have an oscilloscope, it is, of course, preferable to use that for the presetting. Note that the current through the relay coil should not be too high: when a BC 547 is used for T1, it should not exceed 100 mA. That means that the resistance of the coil should be not less than 50 Ω for a supply voltage of 5 V, and not less than 90 Ω at 9 V. The rating of the relay contacts depends on the equipment to be controlled.

Current consumption of the circuit amounts to only a few mA plus the current drawn by the relay coil. For data transfer operation only, the relay is not required: the signals are then taken direct from the collector of T1.

Did you know...?

Robot has come to mean an intelligent and obedient but impersonal machine; it is derived from the Czech *robota* — forced labour. The word robot was first used in Karel Čapek's play *Rossum's Universal Robots* (1920).
(OED)

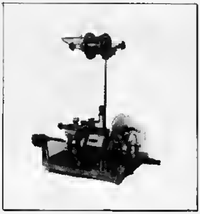
Gain is a ratio, normally expressed in dB. For an amplifier it is the ratio of output power to input power; for an aerial, it is the ratio of the voltage produced by a signal entering along the path of greatest sensitivity to that produced by the same signal entering an omnidirectional aerial. Although often used as such, it is not synonymous with amplification, which is a number indicating by how many times an electronic device increases an electrical signal. Gain is, therefore, 10 or 20 times the logarithm of the amplification, depending on whether that refers to a power or a voltage increase.

NEW PRODUCTS

Coil Winding Machine

Arsun Engineer offer hand operated coil winding machine for winding a variety of coils, using 0.913 to 0.06 mm (20 to 46 SWG) enamelled copper wires. Any type of bobbin square, round or rectangular can be would on the machine. The machines sturdy in construction having mechanical cast iron, brass plate pinion and bevels gears of steel. The shafts are mounted on bearings for smooth running of the machine. The wire from the real is guided by a pulley on reel carrier and two pulleys fitted on the carriage, which is guided on two inverted V ways for high accuracy. The traverse of whole carriage assembly is by means of lead screw and friction mechanism and its direction is reversed manually at the end of each layer by a movement of lever, while the machine is in running condition.

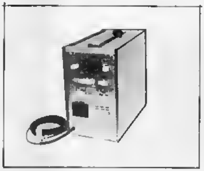
A quick reset type six digit revolution counter is provided for counting the number of turns. This machine is suitable for regular productions as well as small quantity prototype developments, repair shops, technical Institutions and maintenance departments.



M/s. Arsun Engineers • 56/1, Vithalwadi Industrial Estate • Bhavnagar-364 001 (Gujarat).

Digital Vibration Meter

The digital vibration meter V-1103 from Shiken Co of Japan has a charge amplifier input circuit. It offers shock acceleration measurements using Peak Hold performance and random vibration measurements using true RMS calculations, adding to general vibration measurements of acceleration, velocity and displacement. Provisions are made for low cut and high cut filters, and AC DC and digital outputs. As it employs a two-way power supply system of AC and car battery supply, the instrument is suitable for laboratory or field use.



M/s. Murugappa Electronics Ltd. • Agency Division • 29, IInd street • Kamaraj Avenue • Adyar • Madras 600 020 • Phone: 41 33 87 •

Electronically Temperature Controlled Soldering Station.

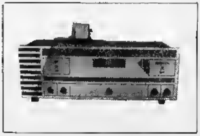
Reliance Electronics offer an electronically controlled soldering station that controls and monitors the temperature of the tip of the soldering iron to the predetermined set value in the neighbourhood of ± 5%. The instrument utilises thyristor power control and the temperature range can be adjusted from 170±C to 450°C. Protection of the tip from voltage spikes and magnetic fields is ensured.

Three-degit LED is provided to know the tip temperature. Compact size, flame-proof skeeving of the solderiing iron, and lightweight soldering iron with iron-coated tips are the features. Operating input voltage can be 230 VAC ± 20%, and output voltage power can be 50 W ± 10%.

M/s. MRK & Brothers Engineers. • 310 A, Commerce House • Nagindas Master Road • Fort • Bombay-400 023•

up Based Digital Printer

Hoshakun have developed a microprocessor based digital printer in two types, one to accept only one input and the other up to 16 inputs. A normal 18 column numeric printer is used to print the date received from outside parameters like temperature pressure, pH, etc. It accepts the signal in terms of D.C. mV/ mA current, any thermocouple or any PRT bulb input. A built-in 5-digit red LED indicates either the measured parameter like °C Dc or the real time clock. The software is user-friendly i.e. after the instrument is switches on, a series of questions will appear on the display, the user is supposed to enter the data, in response to the questions asked by the instrument. For the thermocouple input the linearisation is a standard feature. Printing interval is programmable from 01 minute to 99 minutes. Battery back-up can be supplied optionally. In case of multi-point, the user can state the type of input and the range for each of the input and this can be programmed.



M/s. Hoshakun • Vivek Apparlments • Plot No. 15 • Tulsibagwale colony • Sahakarnagar No. 2 • PUNE-411 009 •

NEW PRODUCTS

Humidity Dry Bulb Temperature Recorder

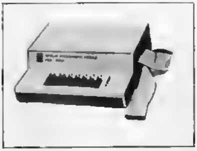
Minicorder-870 combines analogue and digital instrumentation techniques in an instrument to provide both digital display of % RH and dry bulb temperature and strip chart record of the values at 12" hour. The recorder employs latest solid-state sensor. It is housed in an ultra compact cabinet of 144 x 144 mm and recording mechanism consists of only 3 sub-assemblies. The recorder can be commanded to record continuously either relative humidity or dry bulb temperature or alternatively both.

Two displays provide continuous readings of the parameters. Even 15 days of continuous recording is possible. A choice of two types of sensors is available.

Instrument Research Associates Pvt. Ltd. • P B No. 2304 • No. 228 • Magadi Road • Bangalore-560 023 • 350830 355836 •

Programming Module

Professional Electronic Products offors advance Bipolar Programming Module PGM 8530, which can be used with PEP's Universal Prom Programmer PP-85. PGM 8530 is capable of programming Bipolar PROM's of Signetics, National Semiconductor and Texas Instruments. A Comprehensive user manual is supplied alongwith the system for operation of PGM 8530. Some proms of different make are listed which can be programmed through PGM 8530. Signetics 825-23, 123, 126, 129, 130, 131 137, 135, 147, 195, 115, 140, 141, 180, 181, 270, 183, 191, 321 etc. National Semiconductors 74S/54S-188 288, 287, 387, 570, 571, 572, 573, 184, 185, 472, 473, 474, 475, 180, 181, 190, 191, etc. and I. I's 24S-10, 41, 81, 22, 42, 46, 86, 2708, 85, 166, R 165, R45, R85, R166 etc.

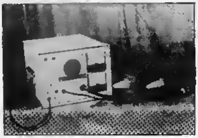


M/s. Professional Electronics Products • Opp. Old Octroi Post • Delhi Road • P.B. 316 • MEERUT-250 002 (U.P.) • Phone: 20460, 20159 •

Breakdown (Flash) Tester

Arun offer a high voltage breakdown (flash) tester for output capacity of 0 to 3 KV, 0 to 5 KV, and 0 to 10 KV with leakage current of 3 to 200 mA in different models. Voltage and current are indicated on two seperate square moving coil type panel meters. Accuracy of measurement is ±5%. A safety measure is the audio-visual alarm devision the front panel when HT is on.

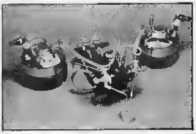
The HV tester is useful for checking breakdown (flash) voltage of insulation material, electrical and electronics components, motors, transformers, switches, chocks, coil, oil, varnishes, relays, etc.



M/s. Arun Electronics Pvt. Ltd. • 2 E, Court chambers • 35 New Marine Lines • Bombay-400 020 • Tel: 259207/252160

Proportioning & Dispensing System

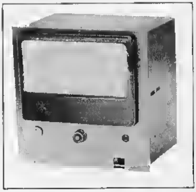
The Model I&J 100 is a proportioning and dispensing system for spoxy, polyester, polyurethane, silicone and other two component resin formulations. Its, features includes: accurate and automatic proportioning and dispensing flowable liquids and pastes; positive displacement piston metering; ratio adjustment from 1:1 to 100:1; pressure feed reservoirs from 6 ounces capacity to 5-gallon; automatic pushbutton dispense switch; and 3-way recharge/dispense valves with air operator actuator.



I&J Fisnar Inc., 2-07 Banta place • Fair Lawn • N.J. 07410 • U.S.A. •

Temperature Indicator/Controller

Hoshakum analogue temperature indicator/controller Type: ATICB-003 is available in range of from 200 to 1600°C with suitable sensors like Cr/Al.Fe/Const. thermocouple and Prt bulb also. Automatic ambient temperature compensation and broken sensor indication are incorporated. The instrument is 230 VAC mains operated and conforms to DIN standard panel cutout.



M/s. Hoshakun • Vivek Appartments • Plot No. 15 • Tulshibagwale colony • Sahakarnagar No.2 • PUNE-411 009 •

NEW PRODUCTS

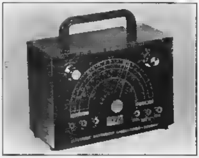
Metallurgical Microscope

Vaiseshika offer the metallurgical microscope Type 7001 to conduct critical examination of metallurgical samples. Optical detection of surface irregularities/inclusions and faults in metals can also be observed with the microscope. The instrument reveals significant specimen details with relief in black and white or brilliant colours. It has achromatic objectives of 10 x and 45 x and wide field eye pieces of 10 x and 15x. These superior optic combinations provide a wide magnification range of from 25 x to 2500 x. Inaddition, coarse and line focusing arrangements enable vertical displacement with 5 micron resolution. Perfect observations are facilitated through optically aligned illumination system. Spring loaded optics offer safeguards against pressure and erroneous operations. Special provision is made for rapid sliding of specimen platform to accomodate bigger specimens. The instrument, is housed in a wooden cabinet; comes with an illustrated instruction manual for complete installation of the equipment with built-in transformer for illumination.

M/s. Vaiseshika Electron Devices • Post Box No. 57 • Near Allahabad Bank • Ambala Cantt-133 001 (India) •

Signal Generator

Equilab Model TP-707 is a solid state AF-RF signal generator covering the range of 420 kHz to 24 MHz in four ranges. It works on 3 V battery. Its simple operation mechanical stoutness and clear scale reading make it suitable, to measure comparative gain and sensitivity in broadcast receiver.



M/s. Electronic Instrument Laboratories • B-69/004, Anand Nagar • Chhatrapati Shivaji Road • Dahisar (East) • Bombay-400 068.

Electronics Maintenance Cleaner

Accra Pac (India), in collaboration with Accra Pac Inc., USA, have introduced the Safeguard Contact Cleaner for electronic maintenance. The cleaner is a specially formulated solvent which restores electrical continuity of all types of contacts and controls. Expceptionally pure solvents under high pressure quickly penetrate surface pores removing grease, dirt, oil and oxidation, and evaporates quickly leaving behind absolutely clean contacts. It is said to have excellent dielectric properties and improve performance and reliability of all electronic equipment.

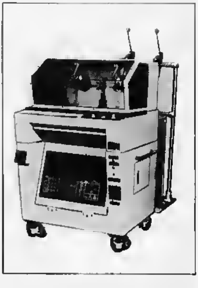
The non-flammable, non-toxic. Safegard Contact Cleaner is useful for silver and precious metal contacts, TV turners, miniature controls, solenoids, circuit breakers, potentiameters, selector switches, volumes and tone controls, relay contacts, thermostat control, distribution panels and all other electronic/electrical contacts.

Accra Pac (India) Private Ltd. • **917, Raheja Chambers • Nariman Point • Bombay-400 021 •**

Coil Winding Machine

The 152NC and 154NC vertical deflection yoke coil winding machine are CNC machines that give flexibility and facilities without compromising on the throughput. The winding specifications can be led into the NC device manually through keyboard retained, and recalled. The rotational axis and axial feed are perfectly synchronised. Feeding and making programmes are simple.

The model 152 NC can wind 2 half coils at a time while 154 NC winds 4 coils at a time. The machine comes with standard accessories like the core chucks and bobbin support devices. The speed of winding can be 1200 RPM. The 152 NC are particulars suited for handling vertical coils of various specifications.



M/s. Muragappa Electronics Limited • Agency Division • 29 IInd Street • Kamraj Avenue • Adyar • Madras-600 020 • Phone: 41 33 87 •

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